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Design of Low Pin Count Scan Architecture

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Abstract- The current trends necessitate high performance DFT techniques to ensure testability of the manufactured SOC. Along with the benefits; these techniques are also accompanied by some costs. DFT scan architectures have power, pin, area and timing requirements, just to name a few. This paper aims in designing and developing a scan control architecture with only 3 I/O pins available. Considering the trade-off with area and test time, the designed architecture must incorporate optimized techniques to ensure no compromise on design controllability and observability. The design is targeted to be compatible with ATPG tool set in order to ensure DFT pattern generation support. Furthermore, the testcase on which analysis is conducted includes sharing these pins are shared with functional pins and hence the isolation requirements are also enumerated. An assessment of the test coverage and area performance parameters is also described to validate the effectiveness of the scan control design. Such technique prove to be a necessity for RFID and MEMs chips were the resource availability for DFT is constrained.

Index Terms-low pin architecture, compressed scan, test wrapper, scan chain**.**

1. INTRODUCTION

Scan is a vital part of any test plan. The main goal of scan is to convert sequential element into a combinational one. This improves the controllability and observability of the design. Even the simplest scan method has basic input requirements. Fullscan requires a dedicated or shared scan input and scan output for each scan channel. To overcome this, compressed scan has been introduced. The main objective of scan compression is to enable access to multiple scan channels using less scan inputs and scan outputs as compared to fullscan. We can lower the pin requirement by increasing the compression ratio. The compression ratio has a trade off with coverage metrics. This means that for a given coverage requirement, the compression ratio cannot be increased beyond a certain value.

The next method introduced for LPCT (Low Pin Count Test) in order to further reduce the pin requirement is adding a macro of cadence called smartscan. Another multisite testing method available is DFTMAX Ultra from synopsys. These methods provide the capability to reduce the pin requirement further to at max a single scan input and output.

In some cases, for example in MEMS and RFID chips, the pins available are limited further. In many cases, the pins available for scan tests may be as limited to 3 to 1 pin. Thus, a custom architecture capable of being controlled by these limited pins without compromising coverage needs to be designed and verified.

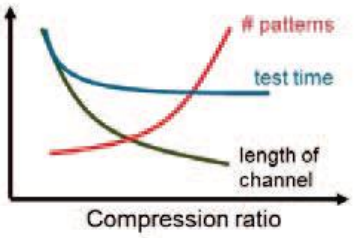

Fig 1 The impact of compression ratio on pattern count, test time and length of channel [7]

2. LITERATURE REVIEW

Our first intention is to understand the challenges and costs of DFT architectures in order to determine which factor we can reduce. Thus, first a review of the existing architectures is necessary. The pros and cons of existing architectures were accessed and we determined the factor where we observed a possible scope of reduction. A brief description of the literature review is available in the following table.

Table 1 Literature Review with Key Learnings

Author	Citation	IEEE Paper/ Journal	Year of Publish	Key Learning
Zhigang Jiang and Sandeep K.	A Test Generat-ion Approa-ch for Systems -on-Chip that use Intellect -ual Property Cores [1]	12th Asian Test Sympos -ium	2003	1.Why ATPG i s difficult for designs with Ips 2.Coars e grain approac h to ATPG 3. Fine grain

				approach to ATPG 4.Comparison of Costs of both approaches in terms of communication time and complexity
Mudasir S. Kawoosa, Rajesh K. Mittal, Maheedhar Jalasuthram and Rubin A. Parekhji	Towards Single Pin Scan for Extreme-ly Low Pin Count Test [3]	31st International Conference on VLSI Design and 17th International Conference on Embedded Systems	2018	Low pin architecture using LBIST
Zhikuang Cai, Kai Huang, Jun Yang	Low Cost Design-for-Testability Features for System-on-Chip: Case Study [4]	2nd International Conference on Computer Engineering and Technology	2010	1.Different mode for analog, MBIST and chain test 2.Comparison of compressed and full scan results
Marcelo de Souza Moraes, Marcos Barcellos Herve, Marcelo Soares Lubaszewski	Low Pin Count DfT Technique for RFID Ics [2]	IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)	2012	1.Design for low pin and low area RFID tests 2.Mixed signal tests
Hyunbean Yi, Jaehoon Song and Sungju Park	Low-Cost Scan Test for IEEE-1500-Based SoC	IEEE Transactions on Instrumentation and Measurement, Vol. 57	2008	1.Basic of IEEE 1500 2.Low pin due to embedded scan enable generation 3.Use of wrapper for at speed testing through pins
Rahul Singhal (Mentor Graphics)	Reduce Test Cost by Combining Low Pin Count Test and Scan Compression	Mentor graphics white paper	2017	1.Use of testcompress for 3 pin DFT (also low power) 2.Use of test controller having 1400 gates for low pin scan

3. INTERNAL TEST SIGNAL GENERATION APPROACH

3.1. Basic Requirements for Optimum scan Design

For any simple scan operation the following signals must be provide:

1. Scan Input
2. Scan Output
3. Scan Enable
4. Scan Clock
5. Scan Reset

In case of limited pin availability, the scan reset can be connected to the POR (power on reset) signal. This may result in limiting the scan reset toggle during

ATPG, but such losses may be neglected for a time being. Also, it is possible to test resets of major critical logic using functional tests.

Next comes scan input and output pins. Since these are essential for controllability and observability of the design, eliminating the requirement of this can be quite tricky. Although an inbuilt random value generation or LBIST sort of structure may be used, these methods come with a heavy toll of area overhead. The next consideration is to determine whether the input and output can be multiplexed. This multiplexing can be achieved using non overlapping scan. This would ensure that data is either shifted in or shifted out at a time, thus avoiding conflict. One limitation associated with this approach is the doubling of test time as the shifting procedure is no long a parallel one. The test time increase is tolerable for small designs will lower flop count as the test time is already lower. In this architecture we will attempt to design the architecture without paying the cost of doubling the test time.

The scan clock needs to be from top-level pin due to unavailibity of on chip clock generation and complex clock controlling units. Thus, comes the consideration to internally generate the scan enable signal. Since the scan enable signal transition mainly depends on the scan chain length for stuck at tests (in order to determine the end of shift operation). Thus, this will be the basis of our proposed architecture. This architecture is simple for stuck at, thus suitable for RFID and MEMs application where transition may not be required due to the high technology node implementation.

3.2. The Design

The scan chain control signals are produced in a control unit called the scan controller. This controlling unit is responsible for the production of various control signals such as the scan mode, scan inputs, scan outputs and scan enable. The available three I/O pins have been assigned the test functionality of scan input (SI), scan output (SO) and scan clock (SCLK). Dedicated registers are assigned in order to bring the chip into test mode using any standard register write protocol. Once the chip enter test mode, the scan controller achieves full control of the test input using the I/O wrapper.

Next, the scan enable must be generated. The scan enable is generated using a counter based approach. The scan length is hard coded into a register inside the scan controller. The counter is initially reset. Once scan mode is configured, the scan enable goes high and the counter is incremented during each clock pulse. The count is compared to the value stored in the register and once both values become equal, the scan enable is held low for a pre-programed duration, calculated based on the scan and capture frequency, after which the scan enable is again held high for shifting again. The period for which the scan enable must be held low is carefully calculated by taking into consideration the timing requirements for scan enable transitions.

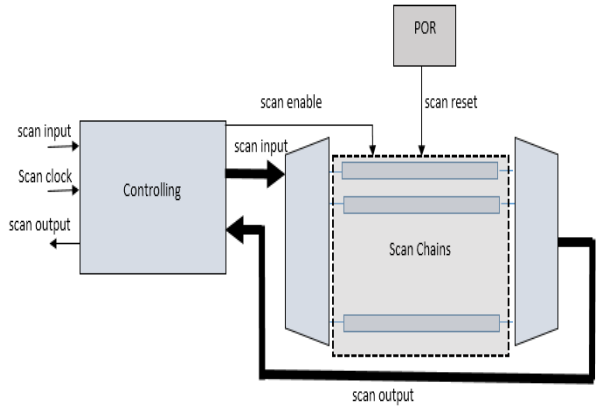

Fig 2 The proposed scan architecture

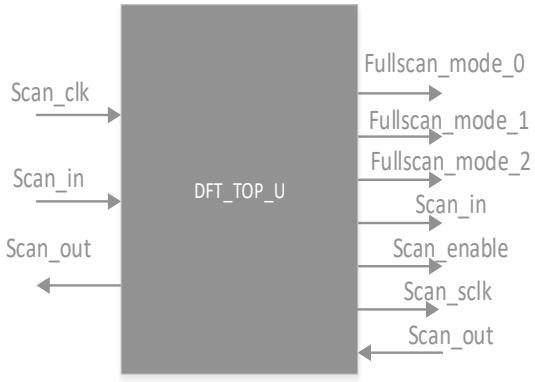

Fig 3 Block diagram of DFT module

A simpler version of the current implementation involves the scan flops to be divided into 3 fullscan chains, each of which is tested separately and exclusively in a serial fashion. The selection of the chain is done based on the test mode register, programmed at the beginning of the test. In order to switch between test modes, the chip must power up and reset again. This results in an increase of the test time.

3.3. The Implementation Flow

Figure 3 depicts the implementation flow. The various verification stages are also included in this diagram.

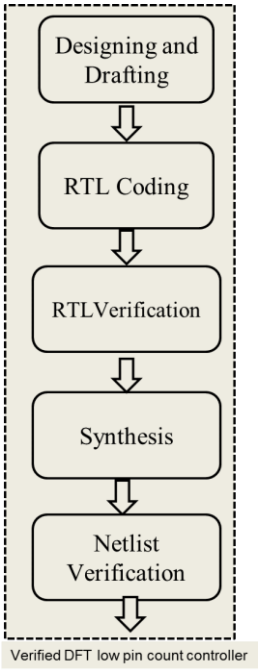

Fig 4 Implementation flow

Once the verification is complete, the functionality of this architecture can be confirmed.

3.4. The Test Wrapper

Since the test pins are shared with the functional pins, this necessitates the need to develop a wrapper to select between scan and function I/O pin operation. This wrapper comprises of multiplexers, selection of which is achieved using the scan mode signal.

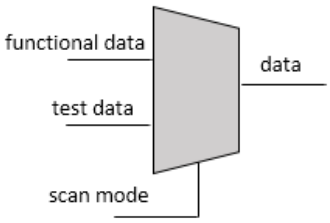

Fig 5 Test wrapper multiplexer

3.5. An Approach to Reduce Test Time

Since the design targeted for implementation has low flop count (~4000 flops), the estimated test time is relatively small, even for a single fullscan chain design. Although for the intended implementation, scan compression method may be applied to further reduce test time. In addition, no additional padding flops are required. The compression-based architecture is shown below:

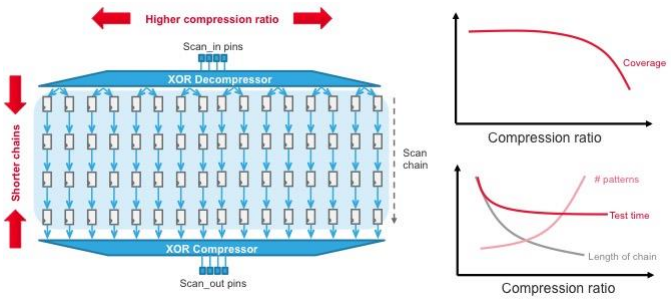

Fig 6 Scan compression technique [8]

4. CAPTURE PROCEDURE HANDLING

4.1. Problem statement

The major issue with a sync counter controlled scan capture Procedure is the need of triggering clock pulses. During flush test, there is no clock pulse for capture and during SSA test capture, there is a single clock to trigger. Thus, a trigger signal is required dictate the change in scan enable signal from low to high.

4.2. Proposed Solution

The simplest solution is to add delay cells. Drawback: delay of delays cells are small in the range of ps and cannot be used when we need such large delay i.e. couple of clock cycles. Since the scan input is not used during the capture this pins function can be multiplexed to perform scan enable change trigger signal during capture and scan input during shift. Special care must be taken for blocking the data to the logic during SSA capture procedure. Otherwise, the logic data near the IOs will be corrupt. For this performing a logical and operation with inverted scan mode signal is used.

5. RESULT

In order to verify the functionality, the RTL code is first synthesized to netlist. A testbench, which provides various stimulus on the three I/O is created. The simulated results showed expected behavior. The waveform of the simulation is shown figure 4.

The scan enable successfully toggles after the counter completes decrementing to the chain length. The dedicated SI and SO is one of the major advantages of this scheme. POR resets the flops initially. The scan control unit requires only 11 flops (including counter registers and configuration registers).

The advantage of this architecture is the ability to execute scan load and unload in parallel, which reduces the test time to half. The scan control unit requires 11 flops (including counter registers and configuration registers). Please note that this value is after optimization. Also owing to the scan design simplicity, easy ATPG using existing vendor tool can be accomplished, which proves to be a major advantage of the design. ATPG tool permits definition of internal scan enable pins and thus same ATPG flow used for multi pin architecture can be used (after making minor modifications). This architecture is

design dependent and the chain length must be reprogrammed to the controller each time there is a change in the scan chain.

6. CONCLUSION

In this paper, we have designed a low pin count scan control architecture after studying the various exiting architectures available. The three pin architecture proposed is based on incremental counter and comparator approach. In addition, we described an approach to reduce test time (if required) using compression. The simulation result showing the scan control operation is also described. The issues encountered and possible solutions are also mentioned.

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(A.1)

Fig 7 Waveform showing the generated scan enable