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Design, Development & Testing of CCD Detector Data Generation & Acquisition System

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Abstract- CCD type detectors are widely used in remote sensing, particularly in applications where low light imaging and higher full well capacity are required. As the requirement of ground spatial resolution increases, the detector output video rate also goes higher and higher. This poses a challenge in designing the video interfaces. Furthermore, the challenges involved in testing such a video interfaces are even higher. The paper proposes a methodology for testing such a detector- video processor interface. The video signal output of the detector is fed into the video processor through AC coupling capacitors, which removes the DC Offset. Further signal is given to the video processor (VP) which performs Correlated Double Sampling thereby removing the Reset Noise. The VP also has a 0dB to 36dB PGA which is adjustable by programming the PGA register and finally performs the Analog to Digital conversion by 12-bit Quantization. The video processor consists the different kind of registers like control register, ADC register, PGA register, CLPDM, SCLK, OE register etc. These registers require various clocks for programming the registers. These clocks are generated using LabVIEW. In addition, the 12-bit data output of the VP is fed to a digital buffer and acquired for further analysis in LabVIEW. The proposed setup is capable of handling video rates up to 12 MHz parallel rate. For a simulated CCD type detector output generated using Arbitrary Waveform Generator (AWG), the setup has successfully demonstrated an SNR of >1000 in 12-bit resolution.

Keywords- CCD detector, data acquisition, LabVIEW, video processor**.**

1. INTRODUCTION

CCD detectors are widely popular in satellite based remote sensing due to their excellent performance in terms of higher full-well capacity, almost 100% fill-factor and high quantum efficiency. When the light reflect on pixels, its convert into electrons & detector is behaved like a capacitor. The output video signal coming from detector is fed into the video processor for conditioning the signal. There are some techniques to reduces the level of noises from signal. However, CDS technique is most efficient technique and video processor consist this technique. A programmable gain amplifier which is constitute of analog & digital stage. The total gain range is 0 dB to 36dB in 0.05dB stage. Programming the PGA register through the serial port, gain can be adjusted. SCLK, SDIN and SLOAD is consent the reading/writing the registers of video processor. SHP & SHD are two clocks which are used to sample the reference and data level of detector signal. A 12-bit resolution and 21 MS/s sampling rate of ADC is converts the analog signal into digital. Now the digital signal is pass to the serializer chip, which converts the 12-bit TTL data into three LVDS data streams. The LVDS data is transfer through LVDS cable to deserializer chip which convert back into 12-bit TTL data. Finally, 12-bit single ended data is transfer to digital I/O board and the data is acquired in LabVIEW through PXI card by using VHDCI (Very High-Density Connector Interface) connector.

2. HARDWARE CONFIGURATION OF THE SYSTEM

2.1. CCD detector output simulation

When the light imitate on the pixels is converted into charge packages. The charge packages are serially shift to Horizontal CCD (HCCD) shift register by via CCD buried channel shift registers. The photoelectrons produced by falling light on pixels is compose by Vertical CCD shift register (VCCD) [10]. Now, signal charge packages are relocated serially to floating diffusion sense node. The floating diffusion sense node is connected to the input of amplifier. A low noise amplifier is converted the charge packages into voltage pulses & producing the output signal voltage on the amplifier output.

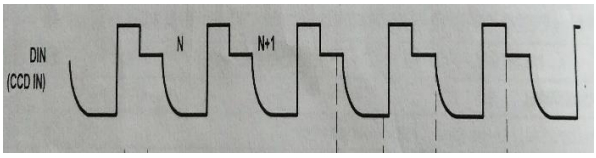

Figure 1. Output signal of CCD detector [9].

2.2. Video processor I/O requirements

The TQFP package of video processor is drives on single 3-V power supply. Video signal generated via PXI function generator is handed to the ac-coupling

capacitor of video processor. The clock rate of video signal is 10MHz.

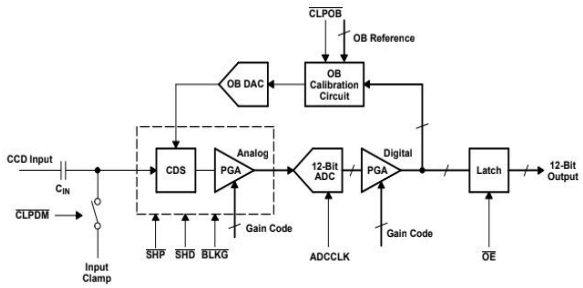

Figure 2. Block diagram of video processor [9].

First the signal is fed into the CDS (Correlated Double Sampling) block of the video processor which decreases the reset noise and further low frequency noises from the signal that are existing on the output of the detector signal. A CLPDM (Dummy Clamping pulse) is clamp the ac coupling capacitor to found the suitable dc bias for the CDS. SHP (Sample Reference) & SHD (Sample Data) registers are used for the sample the reference level of video signal and SHD is used for the sample the data level of video signal [16]. By eliminate the noise from the detector signal, it's passed to the PGA block of video processor. The PGA of video processor contain the gain of 0dB to 36dB and that gain can be control by the programming of PGA register through the serial interface. The video processor consists the read/writes serial registers. A serial register SLOAD (Serial Data Latch), SCLK (Serial Clock) & SDIN (Serial Data Input) serial interface is giving to allow read/write the internal registers of the video processor. Similarly, other register is ADC register used for the produce the proper internal timing using timing generator inbuilt on chip. The internal registers of video processor are reset to their default values by giving the low (logic 0) signal to reset pin. There is software option available to control the reset signal by programming the RTSY register through the serial port. The OB calibration circuit is completely in a closed feedback loop in video processor. OB calibration circuit is clamping the black level of detector signal. Here black level indicated the absence of light. In the absence of light, a suitable amount of current is producing in detector by thermal electrons. A 12-bit, 21-MSPS ADC converts the analog video signal into 12-bit digital output signal. The 12-bit digital output signal is latching with the external pins (D0-D11) of video processor by giving the low signal (logic 0) to the OE pin and if it is high, the buffer is 3-state [9], [11], [13].A 12-bit digital output is onward to serializer chip which converts the 12-bit TTL data into LVDS signal & with the help of 52 pin micro card signals are passed to the digital buffer chip to deserializer chip via LVDS cable. By converting the LVDS signal into 12-bit single ended signal, data is fed into the digital I/O card and output data is acquire in LabVIEW.

2.3. PXI digital I/O board

The 32 pins, single ended digital I/O board is designed by National Instruments. 0-15 pins of I/O board are used for data generation and remaining 16-31 pins are used to acquire the data. VHDCI connector is used to interface between board and PXI digital waveform generator. The registers clock generated in LabVIEW is fed into the I/O board and by using probes of oscilloscope registers clock are display on screen.

2.4. Design methodology of data generation & acquisition system

The CCD detector produce the output signals which is too hard to measure directly with a DAQ device. To protect the DAQ device from noisy signals and high voltages, signal conditioning processor or video processor is mandatory. A video processor amplifies the low-level signals and remove the unwanted signals form data. A 12-bit 21 MS/s digital output is fed into the PXI digital I/O board. Finally, data is transfer through VHDCI connector and acquire in PXI based system. DAQs is calibrating the electrical or physical signal with computer. A DAQs involves the transducers, drivers, signal conditioning processor, A/D converter, communication bus and system with application software as shown in figure 3 [9], [10], [12].

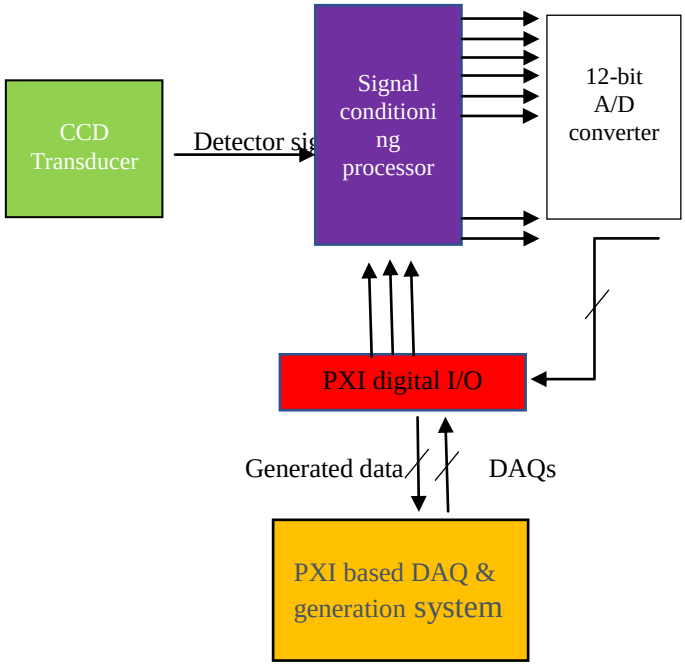

Figure 3. Block diagram of data generation & DAQs.

There are different kinds of registers present in the video processor which perform the specific task. The registers like control register, PGA register, OB register, blanking register, signal polarity register and timing register are required various clocks for programming the registers. These clocks are generated

in LabVIEW. The block diagram of LabVIEW program for data generation is location Find<<examples<<hardware<<NI-HSDIO << Dynamic generation with repeat mode".

Now, the excel file is attached in program which contain the 12-bit of decimal values as shown in the example of excel sheet in Table 1 and Table 2. After compiling the program, a 12-bit of output is coming from PXI bus to digital I/O card.

DIO 5	DIO4	DIO3	DIO 2	DIO 1	DIO 0	Decimal values
SCLK	SLOAD	CLPDM	SHD	SHP	ADC	
0	0	0	0	0	1	385
0	0	0	0	0	0	256
0	0	0	1	0	1	645
1	0	0	1	1	0	550
1	1	0	1	1	1	1527

Table 1.

DIO11	DIO10	DIO9	DIO8	DIO7	DIO6
OE4	OE3	OE2	OE1	SDATA	SDIN
0	0	0	1	1	0
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	0	0	0
0	1	0	1	1	1

Table 2.

Table 1 & 2 is the example of data generated excel sheet.

2.5. 12-bit data acquire by LabVIEW

The full form of LabVIEW is Laboratory Virtual Instrument Engineering Workbench which is completely based on C or C++. The LabVIEW programs are also known as Virtual Instrument (VI) [12]. LabVIEW tool is most widely used for measure, analysis, control, testing, signal generating, acquisition system design, data generating and so many types of operation which we can achieve. The data acquire by LabVIEW is done by using PXI (PCI eXtensions for Instrumentation). There are lots of option to acquire the data like serial, GPIB (General Purpose interface Bus), PXI, PCI, Ethernet, VXI, Image Acquisition (IMAQ), and modular instruments & LabVIEW interconnect in between the hardware to system software by using data acquisition PXI, GPIB, RS232, VXI and RS485. DAQs is calibrating the electrical or physical signal with computer. A DAQs consist the sensors, drivers, signal conditioning, converter, communication bus and system with application software [3], [12].

3. RESULT & DISCUSSION

There are different kinds of registers in video processor which require various clocks for programming the registers. As we can see in figure 5 the output signal of CCD & register clocks of video processor which require to program the registers.

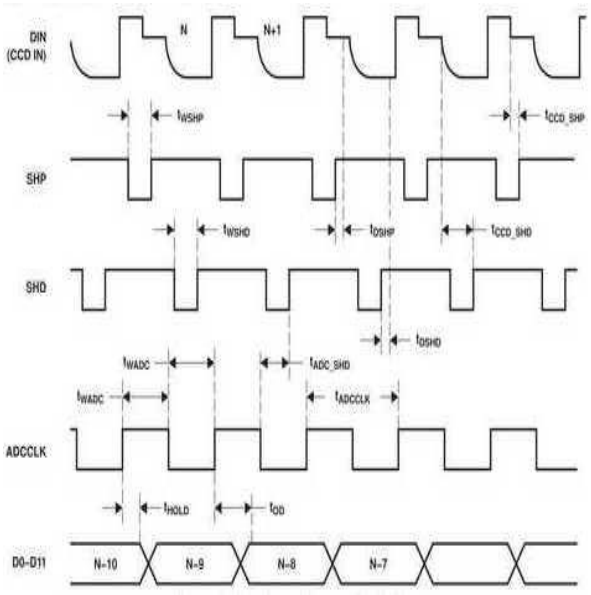

Figure 5. Output signal of CCD & register clocks of video processor [9].

SHP clock. SHP clock is used for the sampling the reference level of detector signal. The other one clock is SHD clock, it is used to sampling the data level of detector signal. Both the clocks SHP & SHD are used for the Correlated Doubled Sampling of video processor. ADC clock is used to latch the output of ADC to the external pins. When the reset signal is drawn low, all the internal registers of video processor is set to their default values. The CLPDM (Dummy clamping pulse), the use of CLPDM pulse is clamp the ac-coupling capacitor to crop the complete dc bias for CDS block of video processor. The serial interface clock is used for the read/write the registers of video processor. The SDIN (Serial data input) clock is 16 bits long. The MSB should be high (logic 1) for read the internal registers & for write the register MSB should be low (logic 0). The OE clock is used for latch the 12 bit of output data to D0 to D11 pins of video processor. By giving the low signal (logic 0) to OE pin, digital data is latched and for giving the high signal (logic 1) to OE pin, the output is 3-state.

4. CONCLUSIONS

This paper designs the data generation & acquisition system of CCD detector. The simulation and the overall system test are carried out. The output result shows the hardware platform and algorithms have completed the data generation & acquisition system. This design is most widely used in remote sensing satellite, industrial measurement, bio-medical and so on.

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