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A Review on Fault Tolerant System for Digital HDL Models

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Abstract- VLSI circuits are complex in nature and Complexity is increasing day by day. Fault tolerant circuits are currently required in several major application. Fault tolerance is a technique which make the system to verify fault. It consist of injecting of faulty input into a circuit and checked the system to find its nature in response to a fault. This is essential method that allow to evaluate the dependence of a system the called fault injection. Fault injection gives capability of fault injection before actual implementation, it helps in determining the testability of digital system. Combinational and sequential digital benchmark circuits are taken under consideration for fault injection and simulation. Simulation of fault gives high controllability and observability of circuit under test. In this paper the fault injection techniques have described.

Keywords- Fault injection, fault tolerance, fault simulation, fault injector, VHDL fault models.

1. INTRODUCTION

A failure have occurred in a digital logic circuit or system if it divert from its actual behavior. The cause and effect of deviations from the desired function of a system are called the factors to dependability. Fault is a unwanted output, lack of perfection, or defect that produce within some software or hardware component. Error is a deviation from actual or desired and is the manifestation of a fault. Failure is the faulty performance of some deed that is expected or due [2].When fault occurred in the circuit it cause an error in output. Sometime the fault remains undetected in the code .Fault can occur during design process. Most of the fault are remove before implementation but some are not removed it reduce a system's dependability when it is hidden into the system. Faults are arises during system operation are classified by their duration: Permanent, transient and intermittent.

- *Permanent faults:* This fault caused by unchangeable component damage create permanent fault.
- *Transient faults:* Due to environmental condition similar as fluctuation in power line, electromagnetic interference or radiation get created.
- *Intermittent faults:* This fault caused by varying hardware or unstable hardware states. By replacing or change in design this faults can repaired.

Fault injection is necessary process for making fault tolerant system Fault tolerant system has additional redundant circuit or system which activate when fault occurred in the circuit and act similar to the circuit which got failed. Fault tolerant system can tolerate one or two fault. Failure in the component causes the redundant circuit activation.

2. SURVAY ON FAULT INJECTION TECHNIQUES AND TOOLS

Testing of the Circuit or System Under Test is tested by applying the proper test set which detect maximum fault. Fault must inject into the system in order to obtaining the maximum fault coverage. There are four kind of fault injection methods.

2.1. *Types of fault injection technique*

2.1.1. *Hardware-based fault injection*

In this method faults are injected at the hardware or physical level. Injector produce voltage or current change and it has actual physical contact with target system. Target system which has not direct physical contact with injector some phenomenon like radiation, interference cause false current inside the target system. It has a little set of injection point. This technique suits best where need high time resolution.

2.1.2. *Software-based fault injection*

The aim of this technique is introducing errors at software level that occurred in hardware level. It can be targeted to applications and operating systems.

2.1.3. *Simulation-based fault injection*

The aim of this method is faults injection at high-level models. It support all system cogitation level. It gives full control of both injection process and fault model. In this method target system and possible hardware fault are model and simulate by software program.

2.1.4. *Emulation-based fault injection*

In this method for fault injection has done by the Field Programmable Gate Array. The main objective of this method is effective circuit emulation and accelerating fault simulation.

2.2. *Design of fault injection technique for VLSI digital circuits*

Lavanyashree B.J and Dr. Jammuna S. [1] proposed an efficient fault injection method to cover all possible fault occurrences and speed up the fault injection. They have taken the two benchmark circuits s27 and Maximally Redundant signed Digit (MRSD) adder

and created fault tolerant system for them with inserting 24 fault at 24 different location. One fault free circuit has taken and it's output response stored in the memory. Another two more copies of test circuit with faults have taken. Result of fault free copy and faulty copies have compare. The proposed demultiplexer based fault injection technique insert the fault in all location and reduce fault injection time. Fault coverage for stuck-at-0, stuck-at-1 and bit flip fault has computed. It is found that bit flip fault has higher percentage of coverage for both circuits.

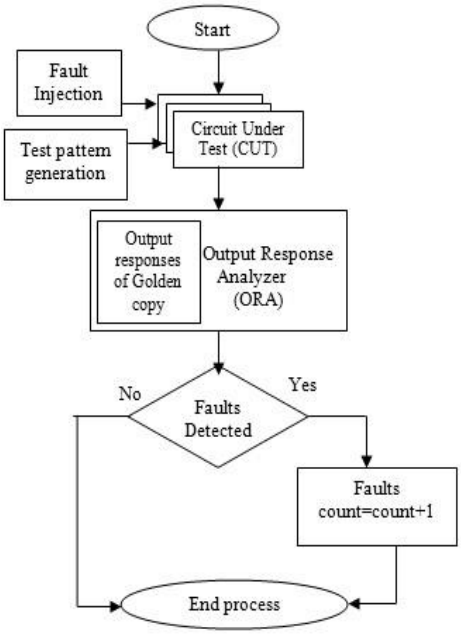

Figure 1: Methodology

2.3. *ATPG method with a hybrid compaction technique for combinational digital systems*

Abdul Rafay Khatri, Ali Hayek, and Josef Borcsok[2] presented demultiplexer based fault injection, activation and selection (FISA) model. In this paper automatic test pattern generation with hybrid compaction technique has implemented. The compaction of test vector using hybrid compaction had done and compared with state-of-the-art methods. In this method fault has injected and tested for three circuit. The hardness of faults is also calculated, and the most sensitive fault locations for all fault models are diagnosed. It helps in increasing fault tolerance of the circuit. Fault coverage value obtained in the range of 87% to 100% in most of ISCAS's 85 circuits. Calculation of fault coverage as fallow,

$$Fault\ coverage = \frac{Number\ of\ fault\ detected}{Number\ of\ fault\ injected} \text{ x } 100\%.$$

2.4. *FPGA-based fault injection into synthesizable Verilog HDL models*

Mohammad Shokrolah-Shrirazi and Seyed Ghassem Miremadi [3] presented the FPGA related fault insertion tool called FITO. FITO is consist of three part.

- Source code updator and fault list generator,
- Fault injection manager
- Result analyzer

The source code modifier are software parts of FITO. Two tools is implemented one is Eclipse editor and other is C programs to insert fault on specific part called checkpoint. In VHDL fault injection manager is implemented. This tool support high speed fault injection process and gives low area overhead. FITO support several fault model gate level and RTL level. Some extra gates and wires are apply for fault injection. Total 4000 faults have been classified accordingly control flow error, data errors and failures error. Survey result show that FITO tool is 79 times quicker than simulation based fault injecting tools.

2.5. *Design and implementation of high speed fault injection process for testing FPGA based design*

Ms. Humera Fatima, Ms. Imthiyazunnisa Begum and D. Naga Poornima [8] has presented high speed fault injection process for creating fault tolerant system. Fault tolerant system is a system or a component which are design such that if the respective system or component fails, it act as a backup component. Author proposed double ALU based fault tolerant system for handling soft errors. For dependability analysis FITO supports several synthesizable fault models. Obtaining good controllability additional gates and wires have added to the original circuit. Speed wise analysis and improvement is carried out with respect to simulation related fault injection method.

2.6. *Transient and permanent fault injection in VHDL description of digital circuits*

P.K. Lala [9] presented a method for transient and permanent fault injection into VHDL level description for sequential and combinational circuit. In this paper fault insertion system is proposed and fault insertion block is included in package body. This technique give freedom to design to access the VHDL package for inserting the fault on any signal within the block of VHDL code. Permanent fault is allow to insert the fault in code at any chosen point called checkpoint. The simple functional call at the starting of VHDL code and component instantiation is require to activate the injection mechanism. In injection system, two linear feedback shift register (LFSR) are used for checking fault insertion into system. Random sequence can be generated with LFSR. Fault injection logic block and One-Hot Encoded shift resister monitor the control inputs to the circuit and determine ether it need to perform transient and permanent fault injection in the data. It also determine on which bit

fault has occurred. The rate of fault insertion is control at control logic block.

2.7. *Simulation based tools for fault injection*

Nowadays digital system is becoming complex and used in the critical and real-time application such as communication, space, medical and automotive application. Therefor there is very large need of evaluating dependability of system. There are many software tools to check dependability of system under insertion of fault.

2.7.1. *FAU Machine*

It is virtual machine and it allow to install operating systems and execute them as independent computer. FAU machine is similar to virtual box [4]. FAU machine support following fault type

- Memory cell
- Disk CD/DVD
- Network

It does not permit the injection of fault in CPU resisters. In FAU machine injection of the fault carried out online through GUI or through VHDL script. This can inject the fault in complete application software or operating system. High simulation speed is provided for complicated hardware and software system.

2.7.2. *Jaka*

It is fault injection tool, it injected the fault in object oriented system and adapted any java application. Java is open source available. Jaka support both low-level and high-level fault injection low level include CPU resister, buses and other.

2.7.3. *LFI*

LFI tool inject the fault at boundary between the target program and shared library. This tool allow to automatically find the shared libraries, recovery codes in program binaries, potentially buggy error, and create corresponding injection scenarios. LIF was developed in response of developing software.

2.7.4. *Xception*

It is used for checking dependability analysis. It uses performance monitoring and debugging to inject the realistic fault. It is low cost tool that can use in large range of processors and machine.

2.7.5. *RIFILE*

It is hardware fault injection tool in which pin-level of fault injection is carried such as the memory, the processor and the bus or other devices [5].It used in the hardware fault injection system.

2.7.6. *LIFTING*

LIFTING is a simulator. It can simulate both logic and fault for stuck at fault [6]. Basic of LIFTING tool is event driven and logic simulator. It support many features for analysis of fault simulation result. It described the hardware system for defining the software stored in memory. Fault insertion can be done in all level elements of hardware model.

3. COMPARISION

TABLE 1. Main advantages and disadvantages of fault injection techniques

Techniques	Advantages	Disadvantages
Hardware-Based	• Location which are hard to access can be access by this method. • For hardware triggering and monitoring it gives high time resolution. • It best serve for the lower level fault models. • Not intrusive. • It provides fast Experiments • Permanent fault can be modeled at pin level.	• It has multiple-chip hybrid circuit, • It has dense packaging, limit accessibility to fault insertion. • It has low observability and portability. • During fault injection it create high risk of damage for the injected system. • It has finite set of injection points and finite set of injectable faults. • It requires special-purpose hardware.
Software-Based	• In near real-time experiments can run. • Not require any extra-purpose external hardware; low complexity, low implementation cost and low development cost. • Model development or determination is not required. • New classes of faults can extended. • Applications and operating systems can targeted.	• It cannot insert faults into checkpoint location that are difficult to software. • To support the fault injection it requires a changes in the source code. • It has limited observability and controllability. • Permanent fault are hard to model. • Limited set of insertion time.
Simulation-Based	• All system abstraction levels can be supported. • It has full control on injection of fault. • It does not need any other special-purpose hardware, it has low cost computer automation. • Maximum amount of controllability and observability. • Not intrusive. • Reliability assessment at different stages in the design process can be allowed. • Both transient and permanent faults can be modeled.	• Large development efforts. • Time consuming. • Model is not easily available. • The goodness of the model used by user, determines the accuracy. • Faults injection at real time is not possible in a prototype. • Model may not include any of the design faults that may be present in the actual hardware.
Emulation-Based	• Injection time is more quickly compared with simulation based techniques. • The experimentation time can be reduced by implanting partially or totally the input pattern generation in the FPGA. These patterns are already known when the circuit to analyze is synthesized.	• It has limited number of I/Os of programmable hardware. • The emulation is only used to assay the functional consequences of a fault. • The price of a general hardware emulation system is more and/or high implementation device complexity of a FPGA based emulation board. • When using a FPGA-based development board, the main limitation becomes the number of I/Os of the programmable hardware. Necessity of high speed communication and the emulation board.

4. CONCLUSION

Fault injection is important process in for creating the fault tolerant system and evaluating the design metrics. Fault injection involve fault insertion and observe its behavior. Faults injection are done at coding phase. Out of the four fault injection technique the simulation based fault injection technique is most popular technique. Using this technique maximum controllability and observability can achieve.

REFERENCES

[1] Lavanyashree B.J and Dr. Jumuna S, "Design of Fault Injection Technique for VLSI Digital Circuits", Second International Conference on recent trends in Electronics Information and Communication technology(RTEICT), May-2017.

[2] Abdul Rafay Khatri, et.al, "ATPG Method with a Hybrid Compaction Technique for Combinational Digital Systems", SAI

Computing Conference, IEEE, July 13-15, 2016.

[3] Mohammad Shokrolah-Shirazi, Seyed GhassemMiremadi, "FPGA-based Fault Injection into Synthesizable Verilog HDL Models" , The Second International Conference on Secure System Integration and Reliability Improvement, IEEE 2008.

[4] Virtualbox.[Online].Available:www.virtualbox .org

[5] H. Madeira, M. Z. Rela, F. Moreira, and J. G. Silva, "Rifle: A general purpose pin-level fault injector," in Proceedings of the First European Dependable Computing Conference on Dependable Computing, ser. EDCC-1. London, UK, UK: Springer-Verlag, 1994, pp. 199–216. Online].Available:http://dl.acm.org/citation.cf m?id=645330.649779.

[6] A. Bosio and G. Di Natale, "Lifting: A flexible open-source fault simulator," in Proceedings of the 2008 17th Asian Test Symposium, ser. ATS '08. Washington, DC, USA: IEEE Computer Society, 2008, pp.35–40. [Online]. Available:http://dx.doi.org/10.1109/ATS.2008. 17.

[7] M. L. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital", Memory and Mixed-Signal VLSI Circuits. Kluwer Academic Publishers, 2002.

[8] Ms. Humera Fatima, Ms. Imthiyazunnisa Begum and D. Naga Poornima, "Design and implementation of high speed fault injection process for testing FPGA based design", International Journal of Science, Engineering and Technology Research, Volumn 3, Issue 10, October 2014.

[9] P.K. Lala, "Transient and Permanent Fault Injection in VHDL Description of Digital Circuits ", circuit and system journal 2013.

[10] Franc Brglez,"Combination profiles of sequential benchmark circuits", IEEE International Symposium on Circuits and Systems ·,June 1989.

[11] Z. Navabi, Digital System Test and Testable Design Using HDL Models and Architectures. Worcester, MA USA: Springer New York Dordrecht Heidelberg London, 2010.