International Journal of Research in Advent Technology, Special Issue, March 2019
E-ISSN: 2321-9637
International Conference on Technological Emerging Challenges (ICTEC-2019)
Available online at www.ijrat.org

Design Of Reversible Rca Using Ns Gate

[1]D.Mahesh, [2]K.Sowjanya, [3]M.Afreen Bhanu, [4]M.Divya Meenakshi, [5]R.Venkateswarlu Naik
[1]*Assistant Professor, Dept Of ECE, Tirumala Engineering College, Jonnalagadda, Narasaraopet, A.P, India*
[2,3,4,5]*B.Tech Scholar, Dept Of ECE, Tirumala Engineering College, Jonnalagadda, Narasaraopet, A.P, India*

Abstract: Design of RCA is basic and most important digital component. At present, one of the most vital issue is reversible logic and this reversible logic has various applications in different areas such as low power CMOS, quantum computing, nanotechnology, cryptography, digital signal processing (DSP), quantum dot cellular automata. A unique one-to-one mapping technique is used in reversible logic gates. To generate a useful function of gate, the reversible gates need some sustained auxiliary inputs. Also for maintaining the reversibility of the circuits some additional unutilized outputs are necessitate that are mentioned to as the garbage outputs. In this paper we design the reversible RCA using NS gate. In this the number of garbage outputs, the number of auxiliary inputs and quantum cost plays a significant role while evaluation. Thus these parameters like area and delay minimizing are most significant for designing reversible circuit efficiently.

KEY WORDS: Reversible logic, Reversible gates, CMOS implementation.

1. INTRODUCTION

For quite a while creative innovation which is quicker, smaller and more complex yet multifarious than its antecedent is being produced. The enlarge in clock recurrence to achieve better speed and improve in number of transistors swarmed over a chip to achieve plan unpredictability of a standard structure results in enhanced power utilization. Around all of the large number of gates utilized to execute logical operations in a regular PC are irreversible. That is, each Time a coherent activity is executed some data about the information is expelled or lost and it scattered as heat. At this junction, it unfolds the need of the reversible logic. Energy loss is a critical factor in present day VLSI structure. Irreversible equipment calculation results in modern VLSI design because of data misfortune. R.Landauer has shown for irreversible logic calculations, each piece of data lost produced KTln2 joules of heat vitality, where K is Boltzmann‟s consistent and T is the temperature at which calculation performed [1-2].

Reversible logic circuit does not have loss of information and reversible calculations in a system can be performed exactly when the structure includes reversible gates. Reversible logic plays a crucial role in the system for the improvement of low power, low loss computational designs which are uncommonly essential for the technique of number math circuits used in quantum count, Nano-development and other low impact propelled circuits. Reversible logic is rising and pulling in thought the progressing past on account of its uniqueness i.e. less heat dissipating characteristics. It has been shown that any Boolean limit can be completed using reversible gates. The normal gates, for instance, AND, OR, and EXOR are not reversible. It might be set up the information data structure from an explicit output model can be exclusively decided. The designed NSG gate can see all Boolean operators. The most basic inspiration driving the proposed framework is that it can work independently as a reversible full adder, reversible full subtractor, reversible half adder, and reversible half subtractor [3].

Boolean logic is said to be reversible if the arrangement of data sources mapped have an equivalent number of yields mapped for example they have coordinated correspondence. This is recognized using reversible gates in the plans. Any circuit having recently reversible gate is prepared for scattering no power. Reversible method of reasoning is commonly used in low power VLSI. Reversible circuits are fit for back-figuring and abatement in spread power, as there is no loss of information. Fundamental reversible gates are used to achieve the required helpfulness of a reversible circuit [4-5]. The uniqueness of reversible justification is that, there is no loss of information since there is adjusted correspondence among data sources and yields. This enables the system to keep running backward and remembering that doing accordingly; any widely appealing setup stage can be by and large broke down. The fan-out of each square in the circuit must be one.

A. Quantum Cost: Quantum cost of a circuit is the extent of execution cost of quantum circuits. Even more precisely, quantum cost is portrayed as the amount of simple quantum undertakings expected to comprehend an entryway.

B. Speed of Computation: The time deferral of the circuits ought to be as low as conceivable as there are various calculations that must be done in a framework including a quantum processor; consequently speed of calculation is a critical parameter while inspecting such frameworks.

C. Waste Outputs: Garbage yields are those yield signals which don't contribute in driving further squares in the structure. These yields wind up excess as they are not required for calculation at a later stage. The rubbish yields make the framework slower; thus for better proficiency it is important to limit the quantity of refuse yields.

D. Input: Looping is entirely precluded when planning reversible circuits.

E. Fan-out: The yield of a specific square in the structure can just drive at most one square in the plan. Subsequently it very well may be said that the Fan-out is confined to 1.

2. BACKGROUND

Gordon. E. Moore anticipated that the quantities of segments on the chip will twofold at regular intervals. At first he anticipated just for a long time however because of development in the coordinated circuit innovation his forecast is legitimate till today. His work is generally perceived as the Moore's law. The impact of Moore's law was concentrated cautiously and scientists have reached the resolution that as the quantity of parts in the chip builds the power dispersal will likewise increment massively. It is additionally anticipated that the measure of intensity disseminated will be equivalent to the warmth dispersed by the rocket spout. Subsequently control minimization has turned into a critical factor for the present VLSI engineers. Landauer expressed that the measure of vitality disseminated to eradicate each piece of data is in any event kTln2 (where k is the Boltzmann consistent and T is the room temperature) amid any calculation the middle of the road bits used to register the last outcome are deleted. This deletion of bits is one of the principle explanations behind the power dispersal.

C. H. Bennett uncovered that the power scattering in any gadget can be made zero or irrelevant if the calculation is finished utilizing reversible model. He demonstrated his hypothesis with the assistance of the Turing machine which is an emblematic model for calculation presented by Turing. Bennett additionally demonstrated that the calculations that are performed on irreversible or established machine can be performed with same proficiency on the reversible machine. The examination on the reversibility was begun in 1980 depends on the above idea. Shor completed a noteworthy research work in making a calculation utilizing reversibility for factorizing substantial number with better effectiveness when contrasted with the traditional figuring hypothesis. After this the work on reversible processing has been begun by more individuals in various fields, for example, nanotechnology, quantum PCs and CMOS VLSI.

Edward Fredkin and Tommaso Toffoli presented new reversible entryways known as Fredkin and Toffoli reversible doors dependent on the idea of reversibility . These entryways have zero power scattering and are utilized as all inclusive doors in the reversible circuits. These doors have three yields and three data sources, thus they are known as 3*3 reversible entryways. Peres presented another door known as Peres entryway. Peres door is likewise a 3*3 entryway however it's anything but a widespread door like the Fredkin and Toffoli entryway. Despite the fact that this door isn't general entryway it is broadly utilized in much application since it has less quantum cost concerning the all inclusive entryway. The quantum cost of the Peres door is 4.

H Thalpliyal and N Ranganatha developed a reversible entryway known as TR door. The principle motivation behind presenting this reversible TR door was to diminish the waste yield in a reversible circuit. H Thalpliyal and N Ranganathan acquainted the reversible rationale with consecutive circuits. Usage of the successive circuit, for example, D-lock, T hook, JK lock and SR lock utilizing Fredkin and Feynman entryway has been finished. After this work more research has been done on consecutive circuits utilizing reversible doors. Utilizing the mix of Fredkin and Feynman entryway another door known as Sayem entryway was proposed by Sujata S. Chiwande Prashanth R. Yelekar sayem entryway is a 4*4 reversible door and is utilized in planning successive reversible circuits.

M.L. Chuang and C.Y. Wang suggested that the quantities of entryways, the quantity of junk yield were diminished in actualizing the Latches and when the outcomes will be contrasted and 25% enhancement was accomplished. Despite the fact that some critical works have been as of now done in the field of reversible consecutive rationale configuration, look into on reversible counters has not been finished. Rajmohan and Dr. V. Ranganathan in actualized counters utilizing reversible rationale.

The synchronous and offbeat counter plans have the applications in building reversible ALU, reversible processor and so forth. This work shapes an essential move in development of expansive and complex reversible consecutive circuits for quantum PCs .

3. REVERSIBLE LOGIC GATES

An gate is said to be reversible if the (Boolean) work it figures is Objective i.e., there is balanced and onto correspondence between its information and yield. A gate is reversible if there is a particular yield task for each unmistakable information. In this manner, a reversible entryway's sources of info can be remarkably decided from its yields. The information vector can be exceptionally decided from the yield vector and the other way around. A fundamental condition is that the circuit has a similar number of info and yield wires.. A necessary condition is that the circuit has the same number of input and output wires. Binary reversible gates compute the logic values 0 and 1**.** Basically, the stored program architecture is given by John Von Neumann, where the each bit is estimated by the process of heat dissipation per Computation. Heat dissipation is obtained by the Destruction of bits as per Landauer Principle. Bannett proposed a Turing machine for loss-less computation by making it reversible. After Toffoli proposed reversible logic gates the development of reversible gates and circuits started. After this various number of gates have been proposed. Two categories are described namely basic gates and generalized gates.

A gate which is reversible can realize a reversible function; computation done by a gate is reversible in nature that means for a gate g the inverse transformation is implemented as gate g-1. Some of the basic gates are given below:

A) **Not gate:** the below figure (1) shows the block diagram of NOT gate. Here A is input and A^1 is output.

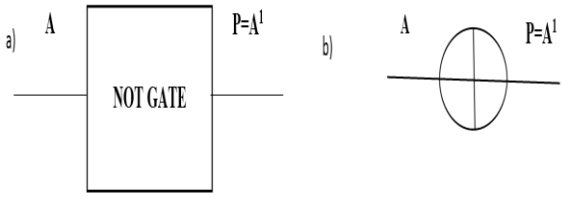

Fig.1: NOT Gate (a) Block Diagram (b) Schematic Representation

Table.1 Truth Table of NOT Gate

Input	Output
A	P
0	1
1	0

B) **Feynman gate** was given by Richard Feynman; it is known as a reversible gate of 2×2. Feynman gate can perform negation operation but in controlled way and this reversible gate is also called Controlled NOT Gate. If two line are A and B, the first line A is known as CONTROL line and second line B is known as TARGET line. Operation on target line is negation and only performed when control line is set otherwise no operation on target line is observed

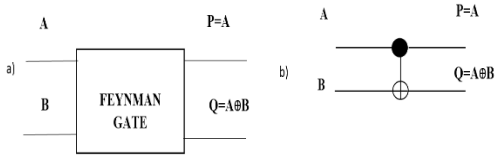

Fig.2: Feynman Gate (a) Block Diagram (b) Schematic Representation

Table.2 Truth Table of Feynman Gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

C) **Toffoli gate:** is a new gate. This gate is known as 3×3 gate and can be generalized up to n×n size. As per definition target line flips when all control lines are set. The block diagram and schematic representation of 3×3 toffoli gate is exhibited in below figure (3).

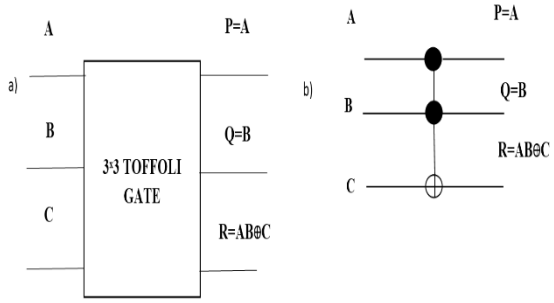

Fig. 3: 3×3 Toffoli Gate (a) Block Diagram (b) Schematic Representation

Table.3 Truth Table of Toffoli Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

D) **Fredkin Gate:** Edward Fredkin and Tommaso Toffoli proposed a new gate called 3×3 Fredkin Gate which is further generalized up to n lines. Figure.4 exhibits the block diagram and schematic representation of new gate called Fredkin gate. If C=0 3×3 Fredkin gate will swaps the values of A and B.

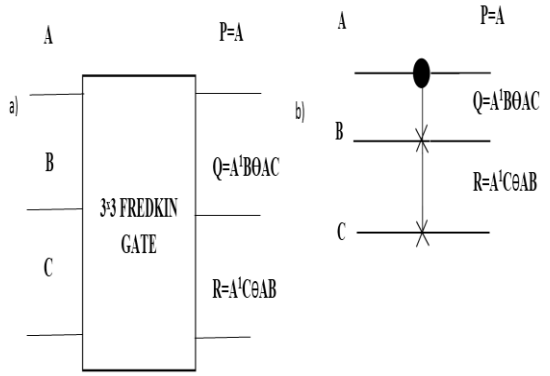

Fig.4: 3×3 Fredkin Gate (a) Block Diagram (b) Schematic Representation

Table.4 Truth Table of Fredkin Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

4. DESIGN OF REVERSIBLE RCA USING NS GATE

The below figure (6) shows the block diagram of reversible RCA using NS gate. The input d, c, b and 0 are termed as input terminal respectively and the output are termed garbage outputs It can be established from the Truth Table that the input pattern analogous to a particular output pattern can be exclusively determined. The proposed NSG gate can perceive all Boolean logical operators. Here the inputs are obtained from memory location and given to NS gate. Since the bits are vast and also ripple carry adder produces all the output values in parallel. The both input and output bits are taken in parallel. The register is taken out or fed back as one of the input to the ripple carry adder.

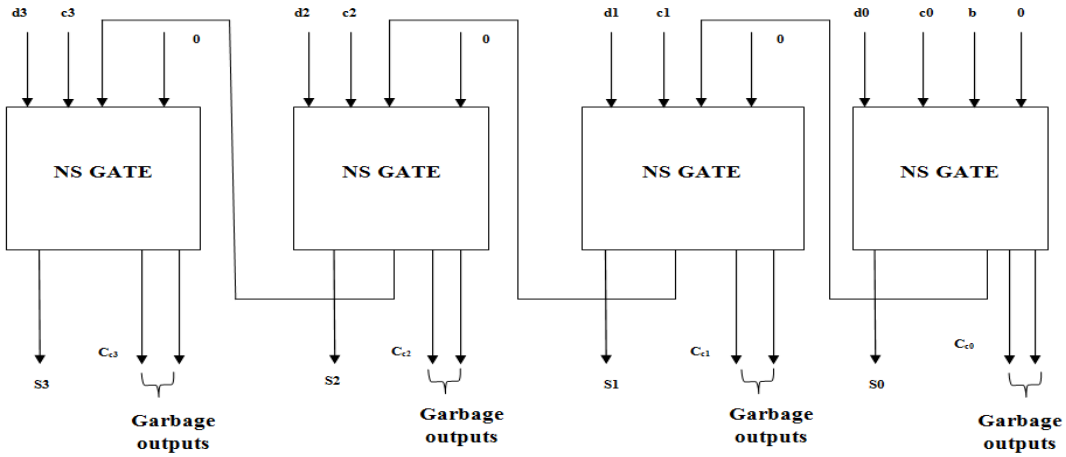

FIG. 6. RCA NS GATE USING REVERSIBLE LOGIC GATES

RCA circuit is intended for addition binary logics. Sum signal (SUM) and garbage outputs are the outputs of the proposed system. Most important arithmetic operation performed almost in all digital signal processors and systems is addition operation. addition is involved in all digital signal and data processing. Thus performance of a system completely depends upon the performance of its RCA unit. The speed, power consumption and area of a proposed system define performance of a system. adders are utilized to implement any operation because these are fast, reliable and efficient components. These are of number of types and depending upon the application a specific type of adder is chosen. In a simple way addition is a process of adding an integer.

Now, the most important and prominent purpose of the proposed gate is that it can work singly as a reversible RCA , A number of reversible adders were proposed. Of all the reversible adder circuits proposed till now, NS gate is better than the previous full-adders designs. The proposed RCA adder using NS Gate requires only one reversible gate (one NS Gate) and The NS Gate produces only garbage outputs while performing operations like full adder,

full subtractor, half adder. Apart from the other reversible gates proposed till now NS Gate can also singly perform the function of a full subtractor, half adder and half subtractor with only garbage outputs.

5. CONCLUSION

Use of the reversible logic gates are increasing day by day but the scientists are still continue with their work on this to further more decreasing environmental decay growth . So mostly we can use this for the power consumption and delay. In this paper we just explained the types of the logic gates and its uses and how we can implement on these logic gates. Basically, we can show the design of reversible RCA using NS gate which will provide low energy consumption and delays are less than its actual circuit design. This unique system can be applicable in multipurpose applications.

REFERENCES

[1] Landauer, R., "Irreversibility and heat generation in the computing process", IBM J. Research and Development, 5(3): pp. 183-191, 1961.
[2] C.H Bennett "Logical Reversibility of computations" IBM J. Research and development, pp 525-532,November 2018.
[3] Raghava Garipelly, P.MadhuKiran, A.Santhosh Kumar "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2017, pp.417-423.
[4] W.D. Pan;M. Nalasani, "Reversible logic", Volume: 24, Issue: 1, IEEE Journals & Magzines Year: 2005 DOI: 10.1109/MP.2005.1405801, IEEE 20016.
[5] Haghparast, M., & Bolhassani, A. (2015). Optimized parity preserving quantum reversible full adder/subtractor. International Journal of Quantum Information, 14(3), 1650019.
[6] Haghparast, M., & Shoaei, S. (2014). Design of a New Parity Preserving Reversible Full Adder. Journal of Circuits, Systems and Computers, 24(1), 1550006. https://doi.org/10.1142/S021812661550006 1
[7] Thapliyal H, Ranganathan N.,"' Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs"' Centre for VLSI and Embedded System Technologies International Institute of Information Technology, Hyderabad, 500019, India, 2013.
[8] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G. Santhi Swaroop ―A distinguish between reversible and conventional logic gates ‖, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2,Mar-Apr 2012, pp.148-151
[9] Thapliyal H, M. B. Shri nivas "Novel Reversible MultiplierArchitecture Using Reversible TSG Gate"' Computer Systems and Applications, 2011. IEEE International Conference on.
[10] C.H. Bennett, ―Logical Reversibility of Computation‖, IBMJ.Research and Development, pp. 525-532, November 2010.
[11] Majid Mohammadi, Mohammad Eshghi, Majid Haghparast and Abbas Bahrololoom, (2008) "Design and Optimization of Reversible BCD Adder/Subtractor Circuit for Quantum and Nanotechnology Based Systems", World Applied Sciences Journal, vol. 4, no. 6, pp. 787-792.
[12] Majid Mohammadi and Mohammad Eshghi, (2008) "Behavioral description of V and V+ gates to Design Quantum Logic Circuits", Fifth International Multi-Conference on Systems, Signals and Devices, pp. 1-6.
[13] Rekha K James, Shahana T K, K Poulose Jacob, and Sreela Sasi, (2007) "A New Look at Reversible Logic Implementation of Decimal Adder", The International Symposium on System-On-Chip.
[14] Himanshu Thapliyal and A P Vinod, (2006) "Transistor Realization of Reversible TSG Gate and Reversible Adder Architectures", Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, pp. 418-421.
[15] Himanshu Thapliyal and M B Srinivas, (2006) "Novel Design and Reversible Logic Synthesis of Multiplexer Based Full Adder and Multipliers", Forty Eight Midwest Symposium on Circuits and Systems, vol. 2, pp. 1593 – 1596.
[16] H Thapliyal and N Ranganathan, (2010) "Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs", Proceedings of Twenty Third International Conference on VLSI Design, pp. 235-240.

[17] Lihui Ni, Zhijin Guan, and Wenying Zhu, (2010) "A General Method of Constructing the Reversible FullAdder", Third International Symposium on Intelligent Information Technology and Security Informatics, pp. 109-113.
[18] Irina Hashmi and Hafiz Md. Hasan Babu, (2010) "An Efficient Design of a Reversible Barrel Shifter", Twenty Third International Conference on VLSI Design, pp. 93-98.
[19] Robert Wille, Daniel Grobe, D Michael Miller, and Rolf Drechsler, (2009) "Equivalence Checking of Reversible Circuits", Thirty Ninth International Symposium on Multiple-Valued Logic, pp. 324-330.
[20] Noor Muhammed Nayeem, Md. Adnan Hossain, Lafifa Jamal, and Hafiz Md. Hasan Babu, (2009) "Efficient Design of Shift Registers using Reversible Logic", International Conference on Signal Processing Systems, pp. 474-478.