International Journal of Research in Advent Technology, Special Issue, March 2019
E-ISSN: 2321-9637
International Conference on Technological Emerging Challenges (ICTEC-2019)
Available online at www.ijrat.org

Design And Analysis Of 4-Bit Vedic Multlier

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Abstract: Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance .The need of high speed multiplier is increasing as the need of high speed processors are increasing . A Multiplier is one of the key hardware blocks in most fast processing system which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction

Keywords- Vedic Multiplication, UrdhvaTiryakbhyam Sutra

1. INTRODUCTION

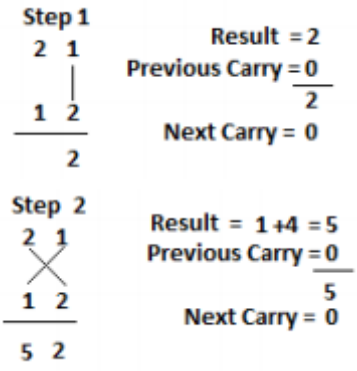
One of the most important block in any processor is a Multiplier. A binary Multiplier is an electronic circuit used in digital electronics. Multipliers are widely used in the field of DSP [14] and image processing which involves multiplication operations, whose performance depends on the effectiveness of the multiplier units. The field of communication involves multiplication of two signals for modulation and demodulation. A conventional multiplier block consists of a chain of AND gates to generate the partial product terms and an adder assembly to add them. The speed limitation associated with the conventional multiplier is due to the latency introduced by long adder tree structures. [7] The power consumption and propagation delay of a multiplier unit is a major design concern. Many researchers have tried to design multipliers which offer either of the following – low power consumption, high speed and hence less area. The use of Vedic Mathematics for multiplication [4] with UT Sutra is applied to the binary number system and is used to develop digital multiplier architecture resulted in significant improvement in the overall speed and power consumption of multiplier.

The paper proposes lower multiplier architectures based on Vedic Mathematics for high speed computing. The proposed 4-bit and 8- bit multiplier architectures based on the UrdhvaTiryakbhyam (Vertical and Crosswise) [3] Sutra of Vedic Mathematic are realized using Verilog coding in Xilinx 14.5

2. URDHVA TIRYAKBHYAM (UT) SUTRA

Veda means knowledge which is a Sanskrit word. Vedic mathematics provide effective computing methods for high speed arithmetic. Veda is rediscovered by the Jagad Guru Shree Bharti Krishna TirthJiMaharaj. According to him the Vedic Mathematics is based on 16- Sutras (algorithm) [3].

The UrdhvaTiryakbhyam (UT) sutras are applicable for all cases of multiplication. The formulae itself is very short and terse, consisting of only one compound word and means “vertically and crosswise”. The use of UT sutra for multiplication reduces the latency of a multiplier unit by introducing parallel computing of partial products. The Multiplication for 2-digit decimal numbers multiplication is illustrated in fig.1



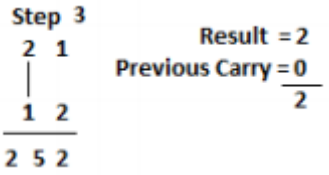


Fig. 1 UT based multiplication for 2 digit decimal numbers

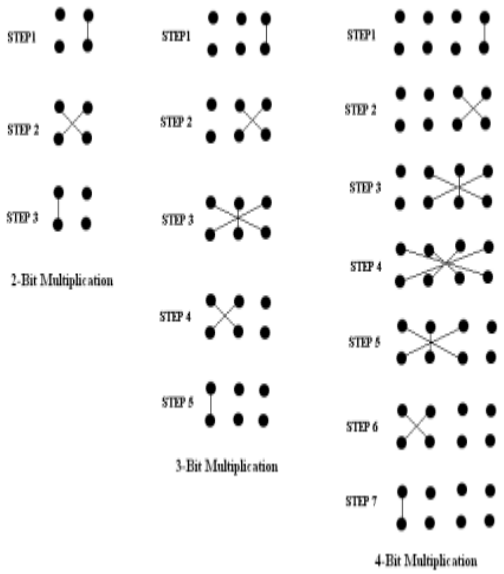


Fig. 2 Line diagram for binary multiplication using UT sutra

In decimal number system, this UT sutra is mostly used for multiplication. However it can be extended to execute binary number arithmetic operations. The line diagram of binary multiplication using UT method for 2-bit, 3-bit and 4- bit numbers is as shown in Fig. 2.

The partial product generation as indicated by the vertical and crosswise lines as shown in the figure is primarily an AND operation. The 2-bit multiplication with two inputs A [1:0] and B [1:0] the following expressions are obtained.

P0= B0A0 (1)

C1P1= B0A1 + B1A0 (2)

C2P2= C1 + B1A1 (3)

Where, BiAj represents the partial product terms for corresponding bit positions i and j of the operands. From partial product addition C1 and C2 are the carries generated and C2P2P1P0 is the result of the multiplication. The 4-bit Multiplication, as shown in the line diagram of Fig. 2, can be carried out by using 2-bit Vedic multipliers [5-10]. Any 4-bit binary number A can be represented as AhAl where Ah denotes the most significant 2 bit positions and Al is the least significant 2 bit positions. A similar concept is used for the number B which is represented as BhBl. Following the same process, two 8-bit binary numbers A and B, represented as AhAl and BhBl respectively, where Ah and Bh are the higher nibbles and Al and Bl are the lower nibbles, can be multiplied using 4-bit multiplier blocks. The line diagram for 8-bit multiplication

3. PROPOSED SYSTEM

4-bit Vedic Multiplier Architecture

4-bit binary multiplier based on the Vedic mathematics can be realized using the UrdhvaTiryakbhyam sutra as explained in the line diagram. All the partial products are generated using a chain of AND gates. The 4-bit binary multiplier can be realized using 2-bit multiplier method. . The paper proposes a novel architecture to implement such a design. This UT based architecture, as shown in Fig.3, uses four 2×2 Vedic multiplier units which ensure a parallel computing approach. Several adder blocks are incorporated in the proposed architecture for addition of the intermediate results generated from the 2-bit multiplier blocks. In this architecture, two 4-bit carry save adder arrangements and one 4-bit vector merging adder are used. The compactness of the design can be incorporated by reducing the hardware requirement; hence the proposed topology ensures an improved performance. The use of high speed and power efficient adder units also provides a significant improvement in the propagation delay and the power dissipation. After one 2-bit Vedic multiplier delay, the least significant two bits of the output are stable whereas the most significant bit of the result is obtained after a larger delay. The exact propagation delay

can be calculated as one 2- bit multiplier delay plus two full adder delays (due to the Carry Save MSB. The ripple carry adder is realized with an assembly of four full adders (14T).

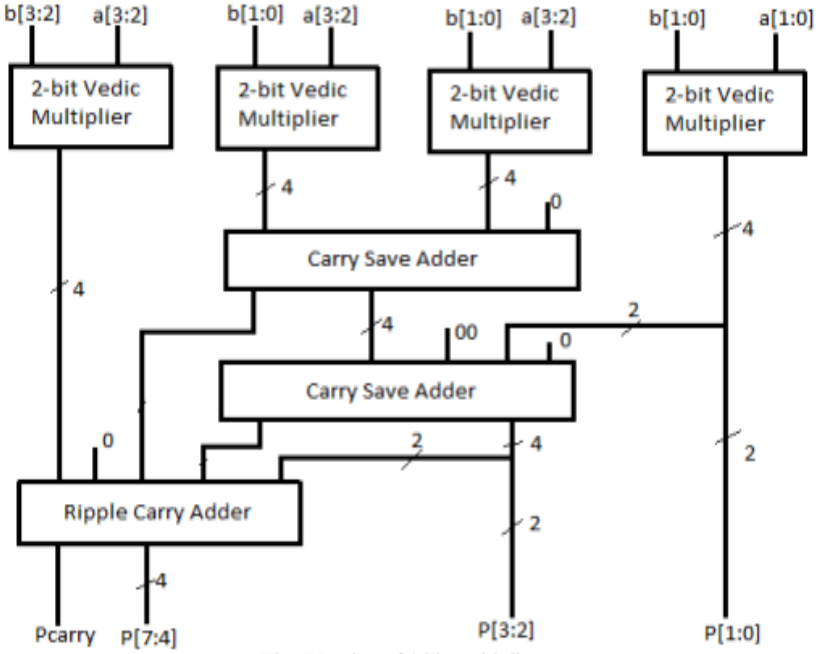


Fig. 3 Design of 4-bit multiplier

4. EXTENSTION

The UT based 8-bit Vedic multiplier presented in this work is as shown in Fig. 8.Design is implemented with four 4×4 multiplier blocks and several adder to realize the proposed topology. The design, presented in Fig.8, is a carry save architecture based on the UT sutra for improvement in overall speed of the topology. Two 8-bit inputs A [7:0] and B [7:0] are multiplied to generate a 16-bit output P [15-0]. The latency is reduced by using adder blocks in the design which are used in a carry save arrangement. The overall propagation delay of the architecture can be estimated as one 4×4 multiplier delay, full adder delays and the delay introduced by the 8-bit ripple carry adder in the final addition stage. The transistor count associated with this design is reduced; however the hardware complexity is justified as it results in an improved performance. The 4-bit multipliers used in the proposed architecture are UT based 4-bit Vedic multipliers as shown in Fig. 6. It can be seen in Fig. 7 that some of the inputs to the carry save adder blocks are given as zero so that uniform bit-lengths for all the inputs to a particular carry save adder stage can be achieved.

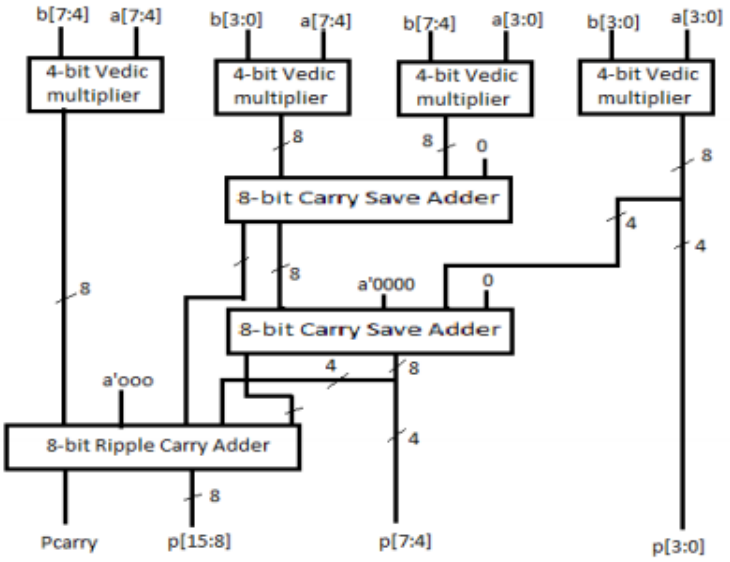


Fig. 4 Design of 8-bit multiplier based on UT sutra

5. CONCLUSION

The paper presents new topologies for 4-bit and 8-bit multipliers based on UT sutra of Vedic mathematics. The topologies are realized in xilinx tool and the performance analysis is performed using several test inputs with a power supply of 0.4 Volt. The multiplier designs proposed in this paper provides improvement in propagation speed and power consumption and the improvement in performance is achieved due to the new UT based architecture with fewer number of adder units. The designs provide less power consumption and high speed computing with the use of low power and high speed adder blocks.

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