International Journal of Research in Advent Technology (IJRAT) Special Issue
E-ISSN: 2321-9637
Available online at www.ijrat.org
International Conference "INTELINC 18", 12th & 13th October 2018

Implementation of Combined Watermarking and Compression Technique Using Fpga

Dr. R. Arunmozhi, Dr. N. Kumaran
[1]*Department of Electical and Electronics Engineering Annamalai University (Deputed to GPTC, Karur) Chidambaram, India, arunau2006@gmail.com*
[2]*Department of Electical and Electronics Engineering Annamalai University (Deputed to GPTC, Karur) Chidambaram, India, kumaran81@gmail.com*

Abstract— The rapid development in the multimedia communication sophisticated the users with many advantages. The two critical needs of this multimedia communication are security and privacy with sufficient bandwidth requirement. The issue of security and privacy of the multimedia data such as image/videos is overcome by employing the cryptographic algorithm and watermarking techniques**.** Similarly, the bandwidth requirement of the multimedia data is cut down by adopting the compression methods. In this research work, the novel idea of combining the watermarking technique and compression technique is introduced. This work employs the Multi-Hybrid Watermarking Technique and SVD based image compression for the proposed communication model. The proposed system is employed and implemented on a FPGA based hardware system using a Xilinx Platform Studio EDK 11.1 FPGA Spartan-6. The proposed system is developed using Matlab for bandwidth computation. Throughout the performance evaluation scenario, the proposed system shows a remarkable improvement.

I INTRODUCTION

The past decade has seen an explosion in the use and distribution of digital multimedia data. Personal computers with internet connections have made the distribution of digital data and applications much easier and faster. However, this has also had a serious effect on copyright encroachment, thereby creating a new demand for copyright protection of digital data[1]. To provide protection for digital data, two complementary techniques have been developed namely encryption and watermarking [2]. Encryption can be used to protect digital data during the transmission process from the sender to the receiver. However, after the receiver has received and decrypted the data, it becomes identical to the original data and is no longer protected. Watermarking can compliment encryption by embedding a secret imperceptible signal, a watermark, into the original data in such a way that it always remains present [3]. Generally, digital image watermarking has certain requirements, the most important being robustness and invisibility.

On the other hand, the transmission of digital information, multimedia data such as, image, and video need moderate bandwidth. The size of the data dominates the bandwidth requirement and also the speed of transmission [4].

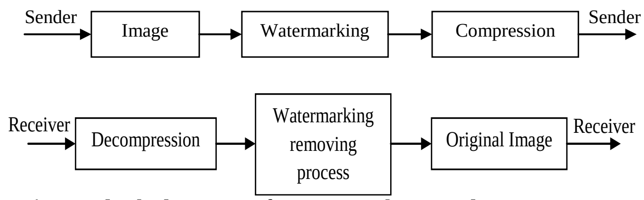


Fig. 1 Block diagram of Watermarking and Compression Method

II PROPOSED WORK

In this work an efficient transmission technique is developed and the term efficient refers to both watermarking and compression of raw multimedia data [5]. The block diagram of the proposed method is shown in Fig.1. In this work, the watermarking of multimedia data is performed using Multi-Hybrid watermarking method followed by a Singular Value Truncating method for multimedia data compression. The watermarking and compression techniques are explained briefly in the preceding chapters. The flow chart of the Hybrid Watermarking and Compression technique is shown in Fig.2.

The steps involved in the implementation of the proposed watermarking and compression method is given below:

Step 1: Input gray image (Size is 512 × 512).
Step 2: Preprocess the original input image.
Step 3: Watermarking process is done by using Multi-Hybrid Watermarking technique.
Step 4: Compression process is made by using Singular Value

Decomposition technique.

Step 5: Watermarked and compressed output image (Size is 512 × 512) is obtained.

Step 6: The watermarked and compressed image is ready to be transmitted.

The steps involved in the implementation of the proposed decompression and removal of watermarking is given below:

Step 1: Input watermarked and compression image (Size is 512 × 512).

Step 2: Decompression process is done by using Singular Value Decomposing technique.

Step 3: Removal of watermarking process is made by Multi-Hybrid watermarking technique.

Step 4: The original image is received (Size is 512 × 512).

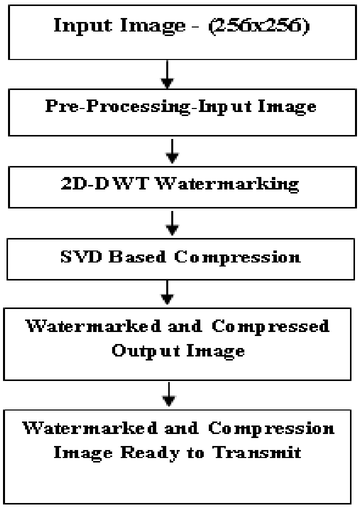


Fig. 2 Flowchart of Hybrid Watermarking and Compression Technique

III FPGA IMPLEMENTATION OF PROPOSED WATERMARKING AND COMPRESSION

In this proposed work the only hardware resource used is SRAM, 32 Bit Micro Blaze Soft Processor and Clock. SRAM is used to store input 512 × 512 gray image and also store processed output image. Proposed watermarking and compression algorithm is developed by using Handel-C HDL with the help of SDK. Developed algorithm is transferred through JTAG cable in the Spartan-6 FPGA to implement the proposed design. Fig.3 shows the automatically generated RTL block diagram for implementation. Embedded Development Kit (EDK) is an Integrated Development Environment for designing embedded processing systems and is shown in Fig.4.

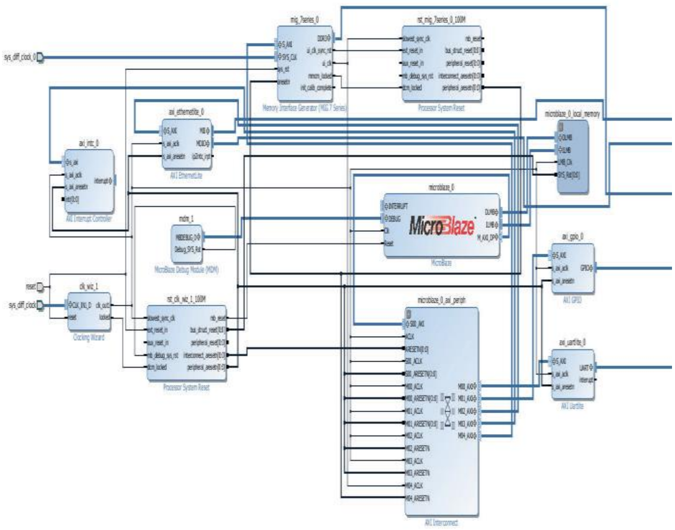


Fig. 3 RTL Schematic Generated for the Proposed Work from EDK Tool

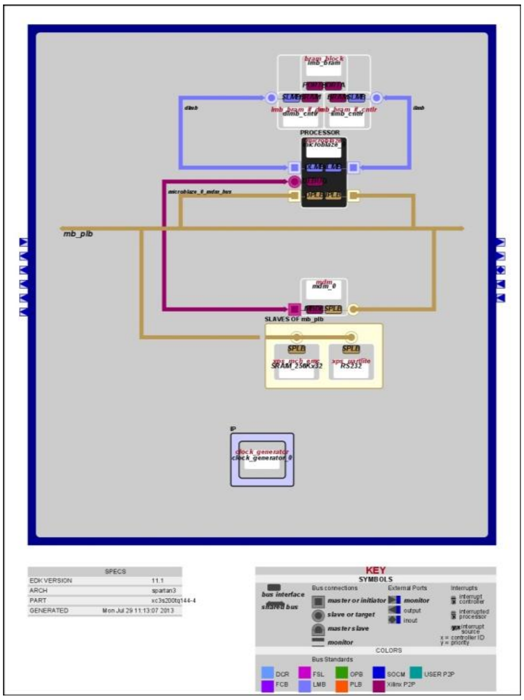
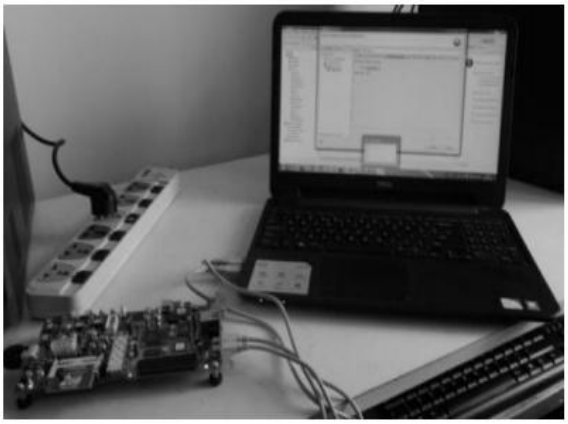


Fig. 4 Micro Blaze Automatically Generated Virtual Processor for Proposed Design

IV INTERFACING SPARTAN-6 WITH PC

The development takes place on one machine (host) and is downloaded to the embedded system (target). For this the Spartan-6 evaluation kit is connected to the PC using USB cables and power on the kit. The external memory card which is of 2GB is inserted at the slot provided on the kit. This external memory card is used to load the input image into the kit, and stores the output image which is a watermarking and compressed image. Fig.5 shows the interfacing of PC with Spartan-6 kit.



Logic Utilization	Used	Available	Utilization
Number of slice Flip Flops	1022	54578	2%
Number of 6 input LUTs	1899	11542	16%
Number of 6 input LUTs	3004	15,032	19%
Total Number of 6 input LUTs	1700	26574	31%
Number used as Logic	890	N/A	N/A
Number used as Shift registers	162	N/A	N/A
Number of bonded IOBs	400	904	44%
IOB Flip Flops	10	N/A	N/A
Number of GCLKs	1	16	6%

Fig.5 Interfacing of Spartan-6 Evaluation Kit with PC

After all the connections are made, FPGA program is clicked on. Here the elf .file and the system.bit file in the Xilinx tool box of SDK is combined into download.bit file which will then be downloaded into FPGA. Prior to download, the instruction memory (FPGA Block RAM) is updated in the bit stream with the executable generation using the compiler[5].

V RESULTS AND DISCUSSION

The efficiency of the proposed method is evaluated in various scenarios. Initially the hardware resource utilization of the proposed system such as number of Flip Flop,6-Input LUT, bonded IOBs, Shift registers, maximum frequency and power is examined by targeting the proposed method in FPGA which are presented in Tables 1 and 2. The bandwidth efficiency of the proposed watermarking and compression algorithm is realized using Matlab. The evaluation made for various images such as, obligatory, teddy, vector field visualization, NEO system, parrots, light field and fisheye effect images are shown in Fig.6.

The proposed image watermarking and compression technique is developed using Handel-C HDL and targeted in Spartan-6 LX9 based hardware system using a Xilinx Platform Studio EDK 11.1 implemented on FPGA board. The hardware resources utilized by the proposed technique for image compression of various images are listed in Table 1. Also, the proposed image technique achieves a maximum frequency of 173.89 MHz at the power rate of 197.61µW which is shown in Table 2.

Table 1 FPGA Resource Utilization

Parameter	Proposed Image Compression	Proposed Image Watermarking
Maximum Frequency (MHz)	173.89	182.34
Power (µW)	197.61	221.35
Processing Time	5.242 ms	

Table 2 Maximum Power and Frequency taken for Proposed Design

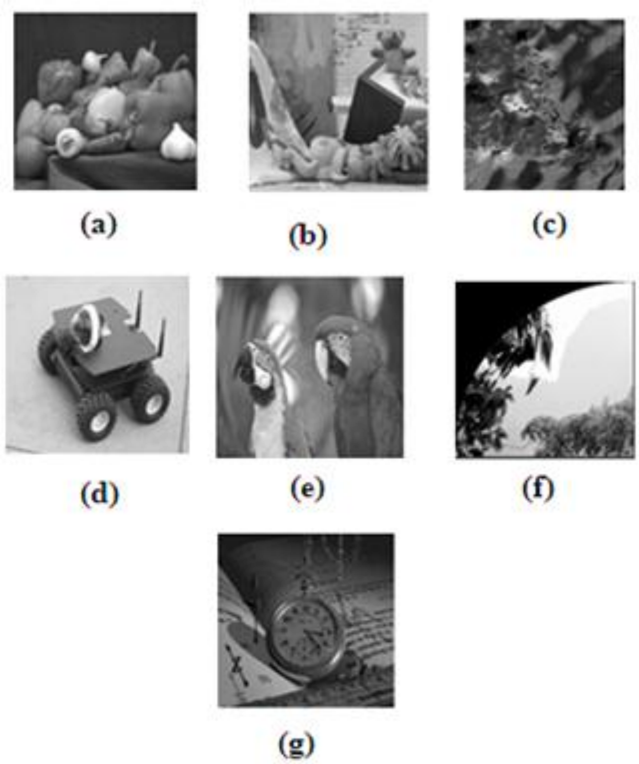


Fig.6 Evaluation of various Images using the Proposed Method (a) Obligatory (b) Teddy (c) Vector Field Visualization (d) NEO System (e) Parrots (f) Light Field (g) Fisheye Effect

Fig.7 shows the comparison between the block size used for compression and the energy consumed for total operation which includes the transmission cost. As the block size is increased linearly the energy consumption increases and hence the compressed image size is increased.

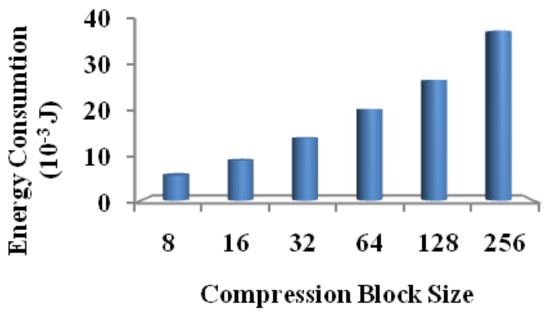
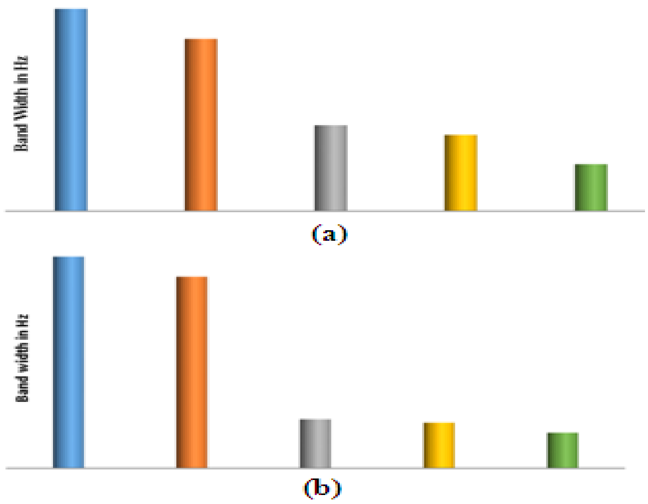


Fig.7 Comparison of Compression Block Size and Energy Consumption

The hardware resources utilized by the proposed method for watermarking are the same as that of image compression. From Table 2, it is inferred that the proposed technique achieves a maximum frequency of 182.34 MHz at the power rate of 221.35 µW. The bandwidth of the proposed system is computed for various images to show its superiority and also the proposed method is realized in Matlab.

Table 8.3 Bandwidth taken by various methods

Images	Comparison of Bandwidth Requirement for various methods				
	LSB	**MSB**	**DCT**	**DWT**	**Proposed**
Obligatory	94	80	40	35.49	21.85
Teddy	86.2	78	20	18.6	14.5
Vector Field Visualization	61	70.89	30	27.5	21.65
Parrots	59	65.35	30.5	25.85	18.85
Light Field	41.5	35.8	25	19.25	10.6
Fisheye Effect	39	24.5	10.9	9.25	7.45
NEO System	27.85	16.75	10.2	8.95	7.05



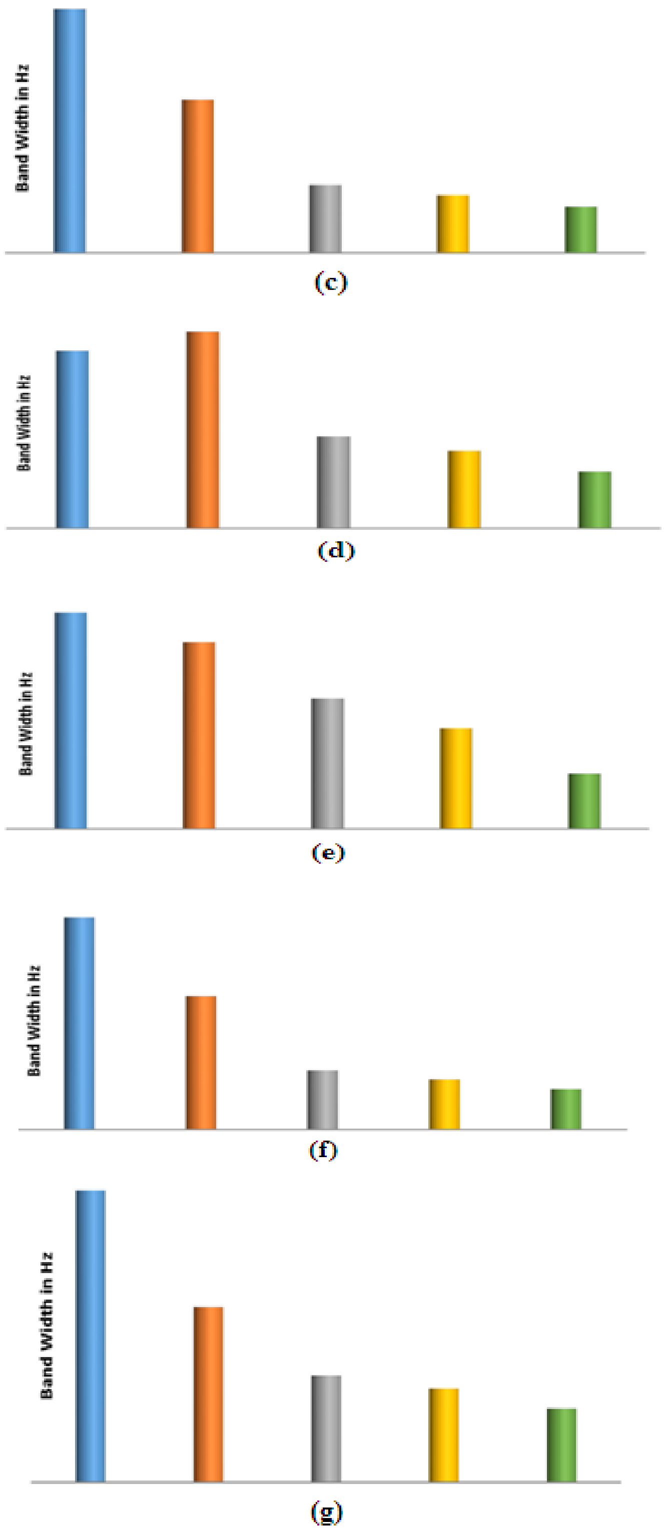


Fig.8 Comparison of Bandwidth Requirement of the proposed method with the Conventional Techniques for various Images

(a) Obligatory (b) Teddy (c) Vector Field Visualization (d) NEO System (e) Parrots (f) Light Field (g) Fisheye Effect

Evaluation is made for proposed image watermarking and compression with the LSB and MSB spatial watermarking technique. Table 3 summarizes the bandwidth requirement for various methods. It is observed from Table 3 that the bandwidth requirement is less when compared to the conventional techniques for various images shown in Fig. 6.

VI CONCLUSION

A novel idea of combining the image watermarking and SVD based compression technique for efficient transmission of data such as an image is presented. The proposed system is developed using Handel-C HDL and implemented on Spartan-6 LX9 FPGA hardware system using a Xilinx Platform Studio EDK 11.1 implemented on FPGA board. It is evident from the results presented that the proposed system is efficient in terms of resource utilization. The time required to market, cost and bandwidth requirement of the system is minimized.

REFERENCES

[1] Rajesh, K. M., Mithun, M., Rahul, S., Venkatkrishnan., Balasubramanian and Vineeth, S, "A comparative study on performance of novel robust spatial domain digital image watermarking with DCT based watermarking" International Journal of Computer Theory and Engineering, Vol. 2, No. 4, pp.1793-8201,2010.

[2] Karthigaikumar, P. and Baskaran, K., " FPGA and ASCI implementation of robust invisible binary image using connectivity preserving criteria" Microelectronics Journal, Vol. 42, No. 1, pp. 82-88,2011.

[3] Yi-Fei Tan and Wooi-Nee Tan,"Image Compression Technique Utilizing Reference Points Coding with Threshold Values" IEEE International Conference on Audio, Language and Image Processing, pp. 74-77,2012.

[4] Zhang, H. and Cao, X., "A way of image fusion based on wavelet transform" IEEE Ninth International Conference on Mobile Ad-hoc and Sensor Networks, pp. 498-501,2013.

[5] Sun, X., Du, J., Li, Q., Li, X., Xu, L. and Li, Y., "Improved energy contrast image fusion based on non sub sampled contour let transform" IEEE Conference on Industrial Electronics and Applications pp. 1610-1613,2013.

[6] Maity, H.K. and Maity, S.P., "FPGA implementation of reversible watermarking in digital images using reversible contrast mapping" Journal of Systems and Software, Vol. 96, pp. 93-104,2014.

[7] Zhai, X., Jing, H. and Vladimirova, T., "Multi-sensor data fusion in wireless sensor networks for planetary exploration" International Conference on Adaptive Hardware and Systems, pp. 188-195, 2014.

[8] Swathi, S., Shobhana, S and Lakshmi, H., "Hardware implementation of watermarking importance and survey" International Journal of Innovative Research in Science, Engineering and Technology, Vol.5, N.10, pp-82-87,2016.

[9] Taha, T.B., Phaklen, E. and Ruzelita, N., "Analysis of Current FPGA Based Image Watermar Attempts" Indian Journal of Science and Technology, Vol.9, No.33,2016

[10] Torres-Huitzil,C., " FPGA-based fast computation of gray-level morphological granulometr " Journal of Real-Time Image Processing, Vol.11, No.3, pp.547-557,2016.