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Survey of Ancient Vedic Mathematics Techniques used in Computer

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Abstract-Knowingly or unknowingly we always use Vedic Sutras in everyday world of technology. As an example, whenever we use i<-- i+1 or i<--i−1 in software routines, we use 'EkadhikinaPurvena' and 'EkanyunenaPurvena' Sutras respectively. Likewise, many Vedic sutras are used in multiplier unit of computer. It will give faster results, which is very much required in various applications like cryptographic algorithms, image processing applications. Traditional methods used for multiplication, division require more time as compared to Vedic methods. UrdhvaTiryagbhyam, Nikhilam sutra are used for multiplication purpose. It require less time, power and give results faster.

Keywords*:* Vedic sutra, UrdhvaTiryagbhyam, Nikhilam Sutra, Dhvajanaka Sutra, Parvartya sutra, cryptography, image processing.

1. INTRODUCTION

Ancient Indian sculptures (Vedas) contain Indian system of mathematics which was rediscovered in the early twentieth century. It includes Vedic mathematical formulae which can be applied to various branches of mathematics. The conventional mathematical algorithms are simplified and also optimized by using vedic sutras. Trigonometry, plain and spherical geometry, conics, calculs are one of few areas where these vedic sutras can be applied efficiently. Now a days, because of increasing demand of digital signal processing, image processing and other heavy computational applications require faster computation by processor. Higher throughput arithmetic operations are required in these signal processing applications. Multiplication, division are one of arithmetic operations which require heavy calculations. Traditional methods for doing these operations take a lot of processing time. These traditional methods include array, booth, carry save, Wallace tree, etc. Multiplier architecture based all these methods are not very efficient in terms of speed, area, power. Vedic multiplication involves fewer steps to solve multiplication than traditional multiplication. This helps to achieve optimization at all levels of design of digital systems reducing power consumption. Vedic mathematics based multipliers are efficient in terms of speed, power and area. In this paper, we reviewed various papers that used vedic mathematical sutras for designing multiplier.

2. RELATED WORK

Surabhi Jain et al. studied vedic mathematics and using that gave binary division algorithm as well as high speed deconvolution algorithm which can be used in image processing. As division is bulky and difficult arithmetic operation, it require higher space and time complexity while implementing on VLSI architecture. They used Nikhilam Sutra and Parvartya Sutra from vedic mathematics for binary division. Their approach shows improvement in time delay as well as complexity [1].

Table 1: Survey of Different Multiplier Design Using Vedic Math

Sr.No.	Title Of Paper	Publisher And Year	Methods/ Sutras From Veda	Features	Language or Tool
1.	Binary Division Algorithm and High Speed Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics)	IEEE-2014	Nikhilam, Parvarty Sutra	Applied For calculating deconvolution, reduced time delay and complexity.	VHDL and Xilinx ISE
2.	Multiplier design based on ancient Indian Vedic Mathematics	IEEE-2008	UrdhvaTiryakbhyam, Nikhilam	Faster multiplier and square architecture, delay and design area less.	ALTERA Cyclone –II FPGA
3.	Vedic Mathematics Based Multiply Accumulate Unit	IEEE-2011	UrdhvaTiryakbhyam	Binary number multiplication, Realized easily on silicon due to regular and parallel structure.	VHDL and Xilinx ISE
4.	Design a DSP Operations using Vedic Mathematics	IEEE-2013	UrdhvaTiryakbhyam	Vedic mathematics based DSP requires less processing time than inbuilt MATLAB functions, Gives better result.	Matlab
5.	Novel Architecture for Inverse Mix Columns for AES using Ancient Vedic Mathematics on FPGA	IEEE-2013	UrdhvaTiryakbhyam, Advanced Encryption Standard (AES)	Low on-chip area and high speed.	Xilinx
6.	High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques	IEEE-2009	UrdhvaTiryakbhyam	Parallel generation of intermediate products	-
7.	Implementation of fixed and floating point division using Dhvajanaka sutra	IJVES-2013	Dhvajanaka Sutra	Used in division of RSA encryption/decryption, efficient in terms of area and speed.	VHDL and FPGA synthesis using Xilinx library
8.	A New Paradigm In Fast BCD Division Using Ancient Indian Vedic Mathematics Sutras	ICCSEA-2013	Nikhilam and Parvartya sutra	The computation time required by the Vedic Division Algorithm is approximately constant irrespective of the size of the dividend.	-

Honey DurgaTiwari et al. gave a multiplier and square architecture for low power and high speed applications. Their approach depends upon ancient vedic mathematical sutras i.e. urdhvatirygbhyam and nikhilam sutra. They showed that nikhilam sutra can be used efficiently for multiplication of two large numbers by reducing it to the multiplication of two small numbers. As compared to booth and array multiplier their approach is more efficient in terms of space and time delay [2].

DevikaJaina et al. proposed a design for multiplier accumulator unit (MAC). The multiplier used in MAC is based on vedic mathematics sutra urdhvatiryagbhyam. Their approach is good for digital signal processing as it require low power. They used VHDL for coding. They compared their approach with modified booth Wallace multiplier and high speed vedic multiplier and found that vedic approach is more efficient than with modified booth Wallace multiplier compared ones [3].

Akhalesh K. Itawadiya et al. identified importance of Digital Signal Processing (DSP) operations and use of multiplication in these operations e.g. convolution, correlation. They gave a simple and easy method for calculating DSP operations for small length of sequences. For this purpose they used urdhvatiryagbhyam, a sutra from ancient vedic mathematics, which is used for doing multiplication. They implemented these operations in MATLAB and showed that this approach require less processing time as compared to inbuilt functions of MATLAB [4].

Sushma R. Huddar et al. identified need of high speed cryptographic algorithm used in secure transactions. To achieve this, they developed an efficient architecture for performing mix columns and inverse mix columns operation. This operation is important in Advanced Encryption Standard method of cryptography. They used ancient vedic mathematic sutra for this purpose and their method gave two times speed as compared to traditional methods used for this purpose [5].

M.Ramalatha et al. designed high speed energy efficient ALU. They used vedic mathematics techniques for this purpose. Their high speed multiplier helps coprocessor which reduces load of processor. They showed that UrdhvaTiryagbhyam method from vedic mathematics is very efficient for multiplication operation. This method reduces unwanted multiplication and produces intermediate results parallely [6].

R. ThamilChelvan et al. gave implementation for fixed and floating point division using vedic mathematics sutra dhvajanka. They showed that their technique is used in RSA cryptographic algorithm. RSA involves division operation and their method using vedic sutra shows greater efficiency as compared to conventional division algorithm. They used VHDL for coding [7].

DigantaSengupta et al. gave algorithm based on ancient vedic mathematics, for fast BCD division.They showed that execution time does not depend upon size of dividend or the divisor but the number of remainders normalization required. Nikhilam and Parvartya sutra are used for division purpose. This approach is faster as it involves addition and negation operations while traditional approach uses successive subtraction methods which are time consuming. But they did not test VLSI implementation of this algorithm [8].

3. CONCLUSION

In this work, we focus on different designs of multipliers which are based on Vedic mathematical sutras. Vedic mathematic sutras are used in place of different arithmetic operations like multiplication, division. They are useful in different applications like digital signal processing, image processing, and computation of heavy calculations. More focus on use of Vedic mathematical sutras used in multiplier will give better results and have a lot of scope in computer field.

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