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An Implementation Of Area Efficient Carry Select Adder Using Cadence EDA Tools Using 90nm Technology

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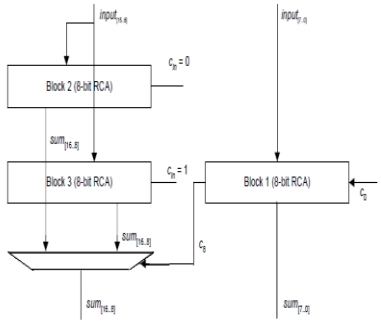
Abstract: In the design of Integrated circuit area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in data-processing processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is reducing the area of CSLA based on the efficient gate-level modification. In this paper a 16 bit, 128 bit Regular Linear CSLA, Modified Linear CSLA, architectures have been developed and compared. However, the Regular CSLA is still area-consuming due to the dual Ripple-Carry Adder (RCA) structure. For reducing area, the CSLA can be implemented by using a single RCA and an add-one circuit instead of using dual RCA. The results and analysis show that the Modified Linear CSLA provides better outcomes than the Regular Linear CSLA. This work is implemented in CADENCE in 90nm technology.

1. INTRODUCTION:

In nearly all digital IC designs today, the addition operation is one of the most essential and frequent operations. Instruction sets for DSP's and general purpose processors include at least one type of addition. Other instructions such as subtraction and multiplication employ addition in their operations, and their underlying hardware is similar if not identical to addition hardware. Often, an adder or multiple adders will be in the critical path of the design, hence the performance of a design will be often be limited by the performance of its adders.
When looking at other attributes of a chip, such as area or power, the designer will find that the hardware for addition will be a large contributor to these areas. It is propagation delay and therefore performs the faster addition operation.
Adding two numbers by using redundancy can speed addition even further. That is, for any number of sum bits we can perform two additions, one assuming the $carry_{in}$ is 1 and one assuming the $carry_{in}$ is 0, and then choose between the two results once the actual carryin is therefore beneficial to choose the correct adder to implement in a design because of the many factors it aspects in the overall chip.
Although adders can be constructed for many numerical representations, such as decimal or excess-3, the most common adders operate on binary numbers. There are various of building adder circuit among that Ripple Carry Adder (RCA) has least complicated circuit but this type of adder is not good for practical use because the speed of addition in RCA is limited by the carry signal that ripples through the adder. In RCA, the sum for each bit position requires a carry from previous stage. Carry Select Adder (CSLA) alleviates the problem of carry known. This scheme, proposed by Kogge-Stone in 1960, is called conditional-sum addition. An implementation of this scheme was first realized by Bedrij and is called the Carry Select Adder (CSLA). The CSLA divides the adder into blocks that have the same input operands except for the $carry_{in}$.

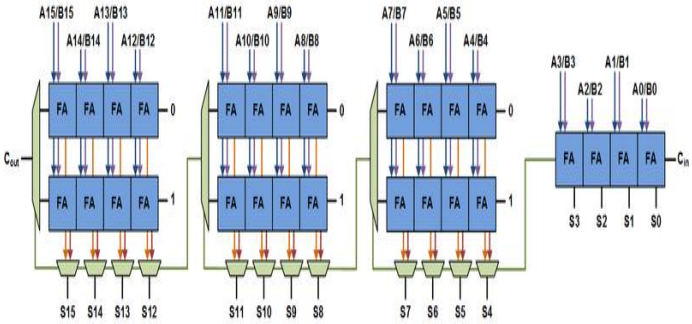
2. BLOCK DIAGRAM OF CSLA:



Block diagram of CSLA

A 4-bit CS adder consists of two (RCA) ripple carry adders and a (mux) multiplexer. The design of carry-select adder is very simple and rather fast. Adding of two n-bit numbers requires two RCA's (two ripple carry adders) and the calculation is done twice ie by assuming the carry being zero and the other assuming as one .

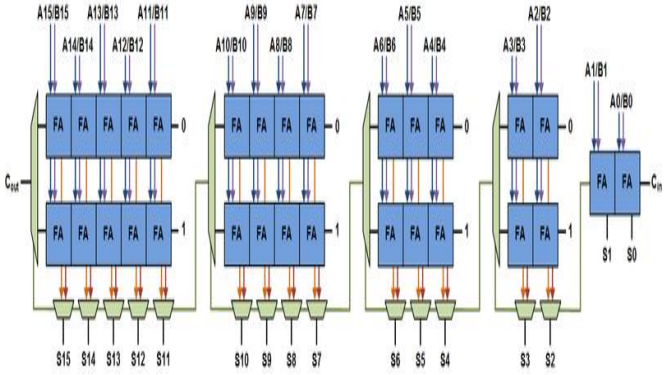
Uniform-sized adder



Block Diagram of Uniform-sized Adder

The above diagram shows a 16-bit carry-select adder designed with a consideration of uniformly sized blocks of 4 and it is created with three of those blocks along with a 4-bit ripple carry adder. In initial state as there is a known carry-in the need of carry select block is eliminated for the first four bits. For the remaining inputs we need the carry select blocks and the delay of the overall adder will be the delay of four full adder delays, along with the delay of three MUX.

Variable-sized adder



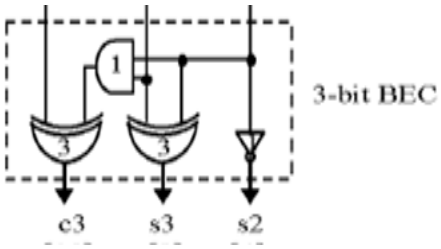
Block diagram of Variable-sized Adder

CSLA uses pair of RCA's, one with carry-in as 0 and other with carry-in as 1, hence the overall delay gets reduced as the propagation delay carry is reduced. Here the major concern is it occupies large area as it requires extra circuitry for calculating the sum and carry with an assumption of 0 and 1 which makes this design less area efficient. To overcome this problem an add-one circuit was introduced by incorporating a BEC. Therefore in Modified Linear CSLA, a Binary to Excess-1 circuit is used.

Binary toExcess Conversion-1

The major design of the area efficient CSLA deals by using a BEC with carry in=1 in order to reduce the area of the regular CSLA, replace the n bit RCA, with an n+1 bit BEC. A structure and the Boolean expressions of a 3 bit BEC are given below.

X0 = ~ (B0)
X1 = (B0 ^ B1)
X2 = (B2 ^ (B0 & B1))



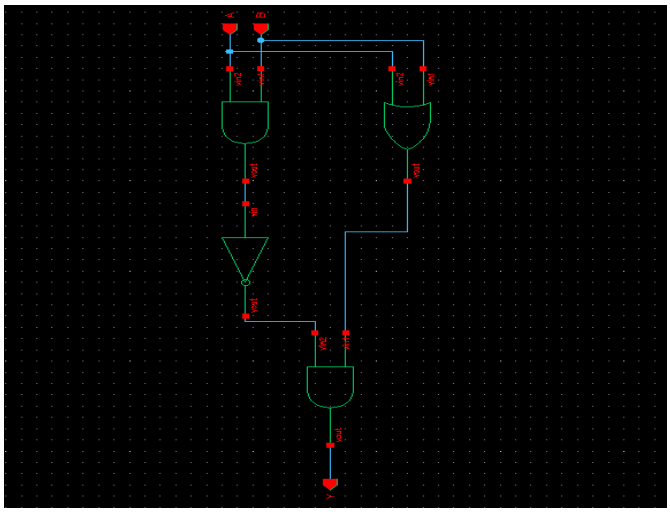
Logic implementation of 3-bit BEC

Truth Table Verification of BEC-1(3bit) is shown below

B[2:0]	X[2:0]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

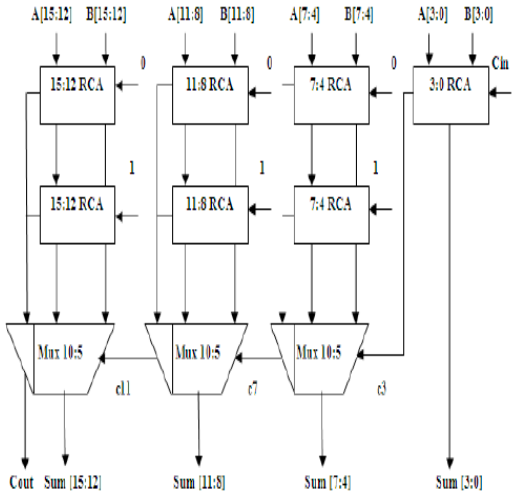
Table: Truth Table Verification of BEC-1(3bit)

The implementation of BEC is shown in below figure. In BEC circuit, it uses XOR gates such that the area and gate count gets reduced. The MUX is needed to select the output of either RCA or BEC based on the value of previous carry given to the select line of MUX.



Logic diagram of BEC

Existing System: Regular Linear CSLA

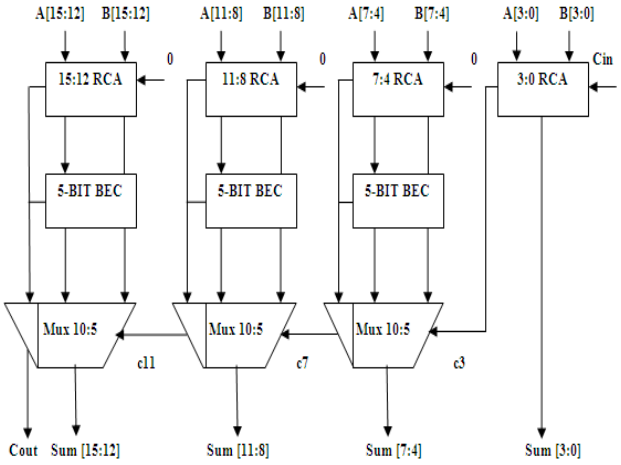


Regular 16-bit linear CSLA

Evaluation of Area of Regular Linear CSLA:
Above module divided into four sets.
Set 1 has only one [3:0]RCA circuit
Set 2 has dual RCA circuits and one [10:5]mux
Set 3 has dual RCA circuits and one [10:5]mux
Set 4 has dual RCA circuits and one [10:5]mux

SET 1:
Each EXOR gate consists of 5 gates, and one full adder circuit have 2 EXOR gates, one OR gate and two AND gates. Total no. of gates required to design a one full adder circuit is = 2*5(EXOR)+2(AND)+1(OR)=13
Proposed Method: Modified 16-bit Linear CSLA

Therefore here we have 4 full adders: 4*13=52 gates.
SET 2:
Total gates required to implement set 2 [7:4]RCA circuit is:
=7F.A+1H.F+1MUX=(7*13)+(1*6)+(5*4)=91+6+20=**1 17 gates**
Similarly gate count of **SET 3, SET 4** are 117 gates as the structure of set2 set3 and set 4 are same it utilizes same hardware.
Total No. of gates required for Regular CSLA is: 52+117+117+117= 403



Logic diagram of Modified 16-bit linear CSLA.

Evaluation of Area of Modified CSLA:
Above module divided into four sets.
- Set 1 has only one [3:0] RCA circuit.
- Set 2 has one RCA circuit, one 5-Bit BEC, and one [10:5] mux.
- Set 3 has one RCA circuit ,one 5-Bit BEC, and one [10:5]mux
- Set 4 has one RCA circuit, one 5-Bit BEC, and one [10:5] mux.

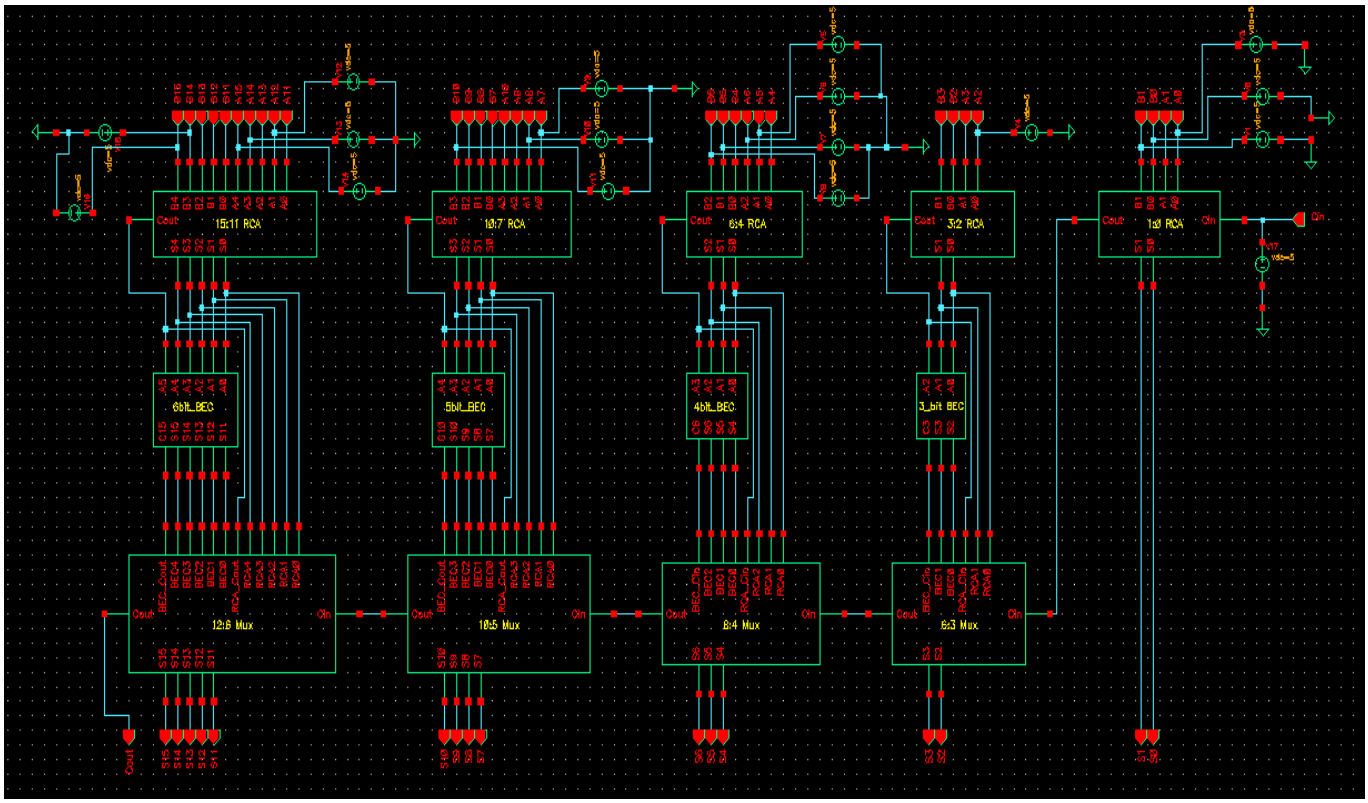
SET 1:
Total number of gates required for this is=4*(F.A)=4*13=52.
SET 2:
Required number of gates to implement set 2 is
=3*(F.A) +1*(H.A) +1*(5-bit BEC) +1*(MUX)
=3*(13)+1*(6) +1*(24) +1*(20)
=39+6+24+20
=89
SET3 & SET4:
The total number of gates required to implement to this is same as set2 hence the gate count is 89.

Therefore, Total No Of Gates Required For Modified 16-Bit Linear CSLA is 52+89+89+89=319.

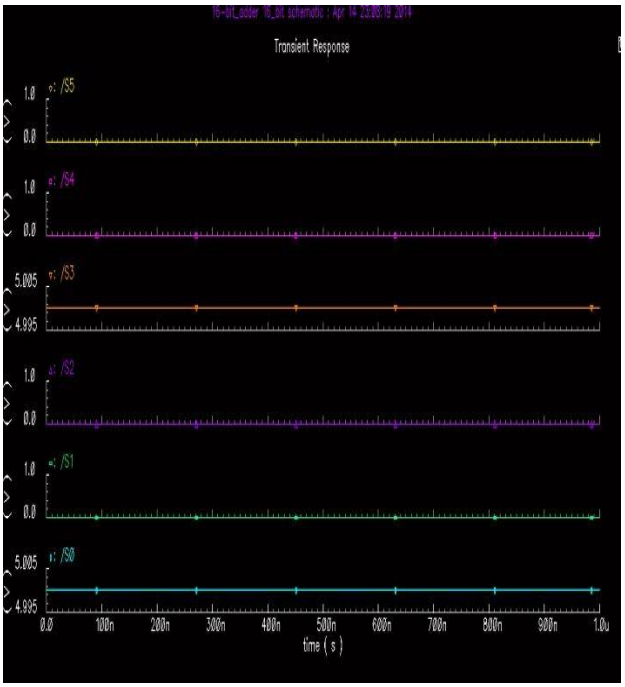
3. IMPLEMENTATION & RESULTS:

The proposed design has been successfully implemented tested and synthesized in CADENCE VIRTUOSO 6.0 software using library of 180nm technology. The schematic of 16-bit Modified CSLA is shown in fig 5 and the corresponding Sum (S15 to S0) and outputs of Carry are shown in fig 6, fig 7 & fig 8.

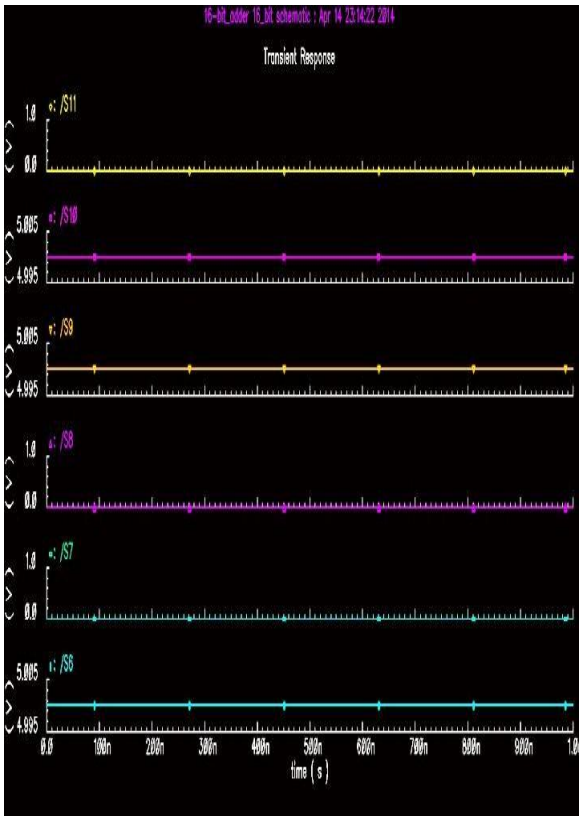
The proposed design in this paper has been successfully tested and synthesized in CADENCE VIRTUOSO 5.0 software using library of 180nm technology. The schematic of modified 16-bit CSLA is shown in fig 5 and the corresponding Sum (S15 to S0) and Carry are shown in fig 6, fig 7 & fig 8.



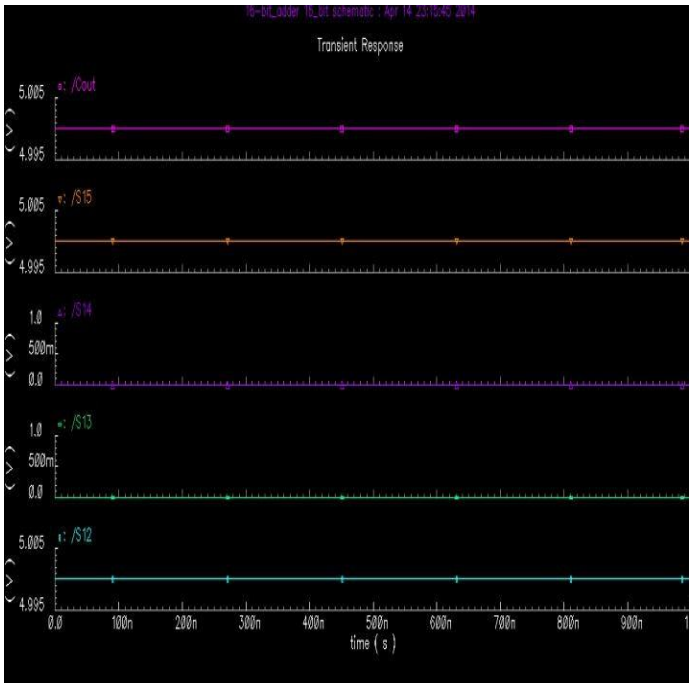
Schematic view of 16-bit modified CSLA



Simulation Waveform (S0 to S5)



Simulation Waveform (S6 to S11)



Simulated Waveform (S12 to S15 and Cout)

4. CONCLUSION & FUTURE SCOPE

An area efficient CSLA is been proposed in this paper by using a modified XOR to reduce the total area and required gate count in modified CSLA architecture. As the total gate count gets reduced the area utilization gets optimized and hence it is useful in terms of area consumption and along with the power consumption too gets reduced. Compared to previous CSLA's architecture the modified CSLA is simple and area efficient. The 16-bit addition operation of CSLA is simulated using CADENCE

VIRTUOSO 6.0 using 90nm technology. The implementation of 32-bit/ 64-bit CSLA would be done and better results can be obtained than Regular CSLA and Modified CSLA. And the design can be implemented further at lower supply voltage and hence the power and area can optimized further.

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