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Design Simulation of Two Bit Multiplier using 90 nm CMOS Technology

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Abstract-In this paper, a binary multiplier is designed using 90 nm CMOS technology for efficient power and area. Binary multiplier is combinational circuits which perform one of the arithmetic operations like multiplication. The three types of designs are proposed as fully automatic, semi-custom, and fully custom. In fully automatic design, inbuilt active devices are used along with auto routing and placement approach. In semi-custom design, inbuilt active devices are used along with optimal routing and placement. In fully custom design, manual active devices are built along with manual routing and placement. In Schematic circuit is designed using gate in the software; layout model is generated when we compile the verilog file. When simulation is completed then the result of auto generated, semi-custom and fully custom are compared on the basis of area and power. After simulation, it is observed that fully-custom is 19.07 % better than semi-custom and 39.81 % better than fully automatic approach in terms of area. In terms of power fully-custom is 52.24 % better than fully automatic and 46.53 % better than semi-custom approach.

Key words- Area, CMOS, Combinational circuits, Layout, Multiplier, Power

1. INTRODUCTION

A binary multiplier is a combinational logic circuit which is used to perform multiplication of two binary numbers. [1],[2]. The output of a combinational circuit is depending only on the present input or the output of a combinational is determined on the basis of the present input. If multiplication is compared with addition and subtraction, multiplication process is complex in nature as compare to addition and subtraction. In the process of multiplication number which is multiplied by another number is known as multiplicand and the number multiplied is known as multiplier.[1],[3]. The binary multiplication is very much easy as compared to another multiplication because it contains only 0s and 1s. [1], [4]. The four basic rules which are used in binary multiplication are:

1. 0 X 0=0
2. 1 X 0=0
3. 0 X 1=0
4. 1 X 1=1

The binary number can be multiplied with different method named as partial product addition and shifting, and using parallel multipliers. [5], [6]

VLSI stands for Very-large-scale-integration. VLSI is a process to generate an Integrated circuit by using thousands of transistors with in a chip. Before the introduction of VLSI technology, most ICs had a limited functionality. ICs have three key advantages over digital circuits viz. size, power consumption and speed. So far several technologies have been used to design binary multiplier cell to improve area and power consumption. For working on these parameters we use different technology such as 45 nm CMOS Technology, 90 nm CMOS Technology, 180 nm CMOS Technology etc.

2. BINARY MULTIPLIER

A binary multiplier is a combinational logic circuit. Binary multiplier can be implemented with the help of AND gate and Half adder. [8]- [11]. Half adder can be design with the help of XOR gate and AND gate. [12] - [14].

Two types of operations perform in case of binary multiplication:

1. Multiplication of two digits for generate partial product.
2. Addition of these partial products with or without carry. [11],[15].

Basic circuit diagram of two bit multiplier is shown below in Fig. 1.

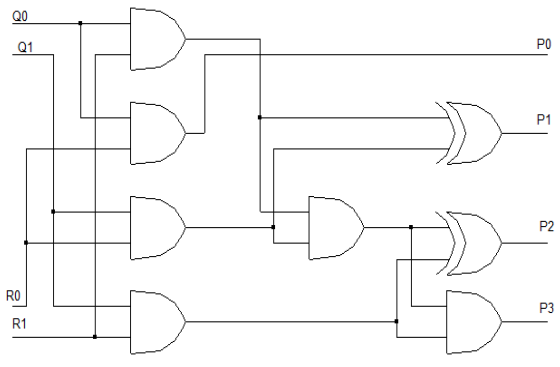

Fig. 1. Two bit binary multiplier

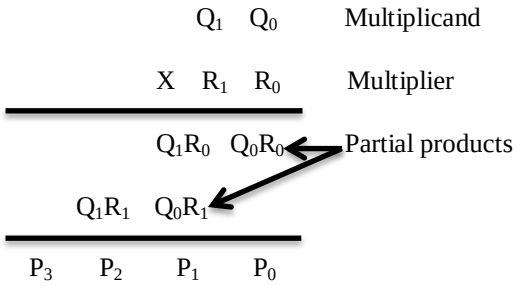

Fig. 2. Two bit multiplication

For perform multiplication operation we need multiplicand and multiplier. Process of multiplication is shown in Fig. 2. Here Q_1 and Q_0 shown as multiplicand and R_1 and R_0 shown as multiplier. When we perform multiplication then Q_1R_0, Q_0R_0, Q_1R_1 and Q_0R_1 partial product are generated. After adding these partial products final result came.

Where

$P_0 = Q_0R_0$ $P_1 = Q_1R_0 + Q_0R_1$

$P_2 = Q_1R_1 +$ Carryout of P_1 $P_3 =$ Carryout of P_2

The equation of a multiplier is shown below. In this equation P denotes the final product which is generated after partial product addition. Q denotes multiplicand, R denotes multiplier, i denote the range of multiplicand and j denotes the range of multiplier.

$$P = \left(\sum_{j=0}^{M-1} Q_j 2^j\right)\left(\sum_{i=0}^{N-1} R_i 2^i\right) \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$P = \sum_{j=0}^{M-1}\sum_{i=0}^{N-1} Q_j R_i 2^{i+j} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

For two bit multiplication the value of i and j is (0, 1) and the value of M, N is 2 in the equation which is shown above. Example 1 of 2 bit binary multiplier is shown in Fig. 3.

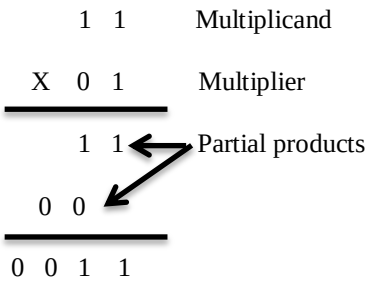

Fig. 3. Example of Two bit binary multiplication

3. SCHEMATIC DESIGN

The schematic diagram for two bit binary multiplier which is shown in figure 4 is generated with the help of DSCH software. After multiplication partial products is generated using AND gates and generated partial products are added using half adder to produce the result. [12]. For providing input to the multiplier we use Buttons and for checking output we use LEDs in the software. In the gate level schematic we design half adder using only NAND gates because half adder design using NAND gates required 10 pMOS and 10 nMOS. If we design half adder using XOR gate and AND gate then we required 11 pMOS and 11 nMOS. The schematic design which is generated with the help of software is shown in Fig. 4. If we simulate the gate-level schematic of two bit binary multiplier according to example which is shown in Fig. 3, then the simulated result of schematic two bit binary multiplier is shown in Fig. 5.This simulated result can be verified with the help of truth table of two bit binary multiplier which is shown below as Table 1. or the timing diagram of two bit binary multiplier which is generated by software shown in Fig. 6.

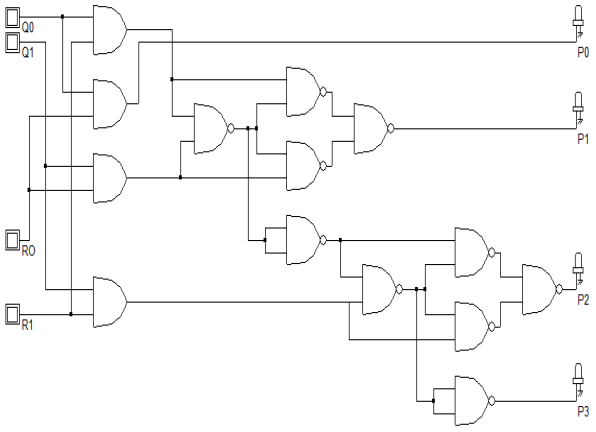

Fig. 4. Gate-level Schematic of binary multiplier

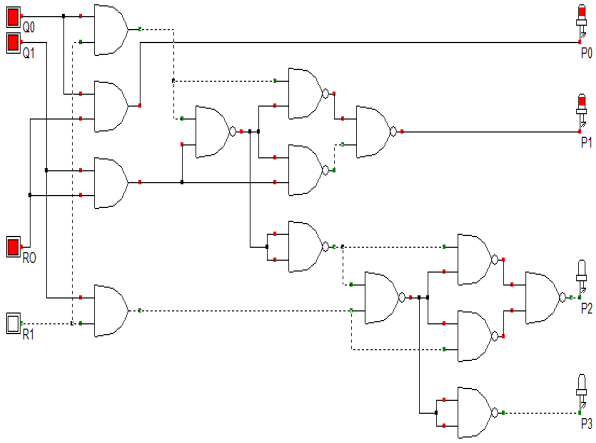

Fig. 5. Simulated result of schematic binary multiplier

Table 1. Truth table of two bit binary multiplier

INPUT				OUTPUT			
Q_1	Q_0	R_1	R_0	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0

0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

The Timing Diagram of two bit binary multiplier which is generated by software is shown in Fig. 6. Timing diagram of a two bit binary multiplier is also verified with the help of truth table of two bit binary multiplier which is shown above in Table 1.

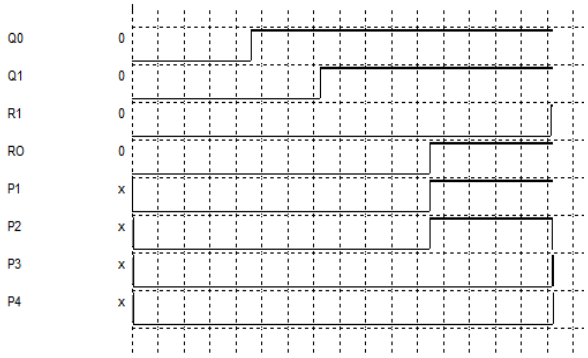

Fig. 6. Timing diagram of two bit binary multiplier

4. LAYOUT DESIGN & SIMULATION

For layout design and simulation different approach is used. Here we used fully automatic, semi-custom and full-custom design approach .The first method is fully automatic design which used inbuilt active devices along with auto routing and placement approach. In schematic of binary multiplier is designed using DSCH software and generate a Verilog file. Using microwind software compile Verilog file which is generated by DSCH software. Then two bit binary multiplier automatic layout is generated and selected CMOS 90nm foundry. The Fig.7. shows this binary multiplier fully automatic layout design. Timing diagram of fully automatic binary multiplier layout design consist many input and output waveforms which is verified by comparing the circuit operation. Fig.8. shows the timing diagram of automatic generated layout.

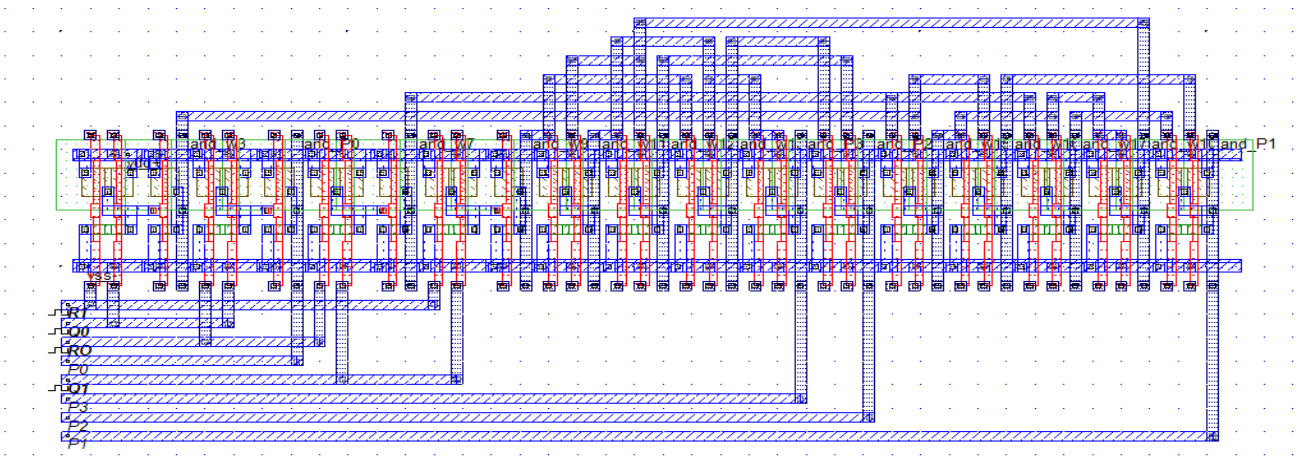

Fig. 7. Fully automatic two bit multiplier layout

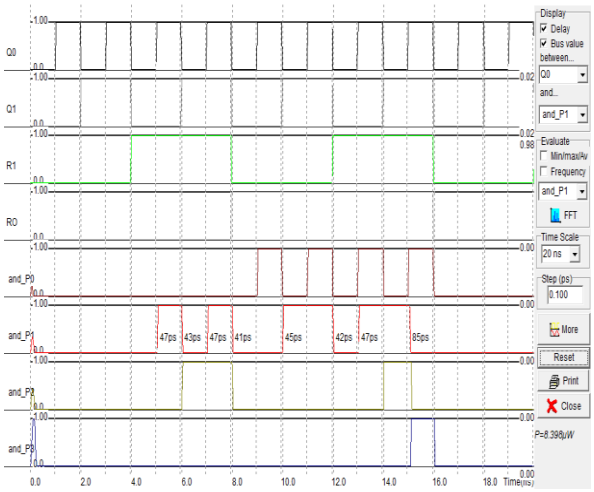

Fig. 8. Timing Diagram of fully Automatic Layout

The layout area, number of pMOS, nMOS used in the circuit is measured from the properties. We measure the consuming power 8.398 µwatt by this layout simulation, and the layout area is measured from the properties. Area required for this particular layout is 181.1 µm². Width is 20.9 µm and height is 9.0 µm. From the electrical properties we note that 39 electrical nodes are used, 32 pMOS devices are used and 30 nMOS devices are used. In second method we prepare layout with the help of semicustom approach. In semi-custom design, inbuilt active devices are used along with optimal routing and placement. In semicustom approach transistors (pMOS, nMOS) are inbuilt in the software. In this approach gates, modules and circuits are design with the help of these transistors by follow the lambda design rule. Using this approach there is a possibility of power reduction or area reduction. Fig.9. represent the semicustom layout.

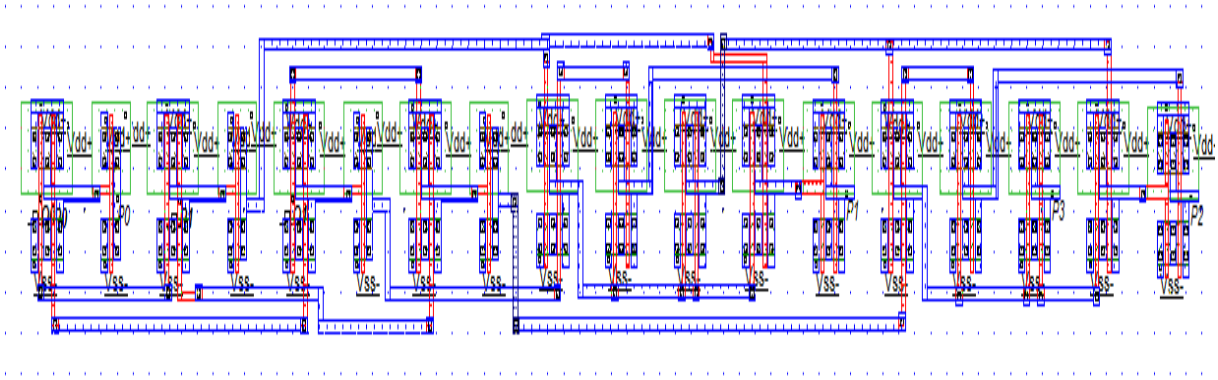

Fig. 9. Two bit multiplier Semi-Custom layout

This layout is checked for DRC if there is no error then it is simulated, and timing diagram of automatic layout is generated. Timing diagram consist many waveforms which is verified by comparing the circuit operation. Fig.10. shows the timing diagram of automatic generated layout. We measure the consuming power 7.815 µwatt by this layout simulation, and the layout area is measured from the properties.

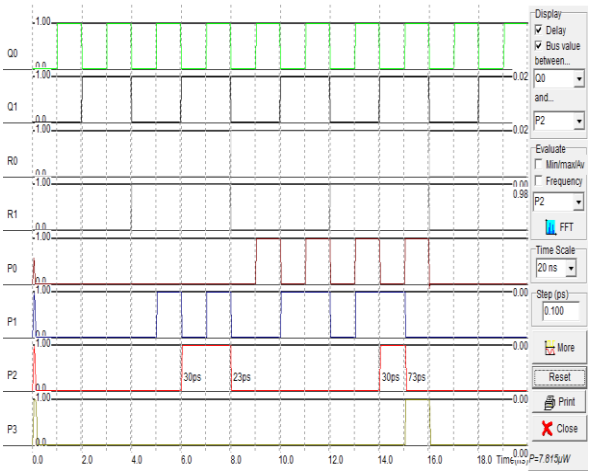

Fig. 10. Timing Diagram of semi-custom layout

Area required for this particular layout is 134.7 µm². Width is 36.9 µm and height is 3.7 µm. Area and

power both are reduced in semicustom design as compared to fully automatic design. From the electrical properties we note that 91 electrical nodes are used, 32 pMOS devices are used and 30 nMOS devices are used in semi-custom layout design. The layout area, number of pMOS, nMOS electrical nodes used in the circuit is measured from the properties.

In third method we prepare layout with the help of fully custom. In fully custom design, manual active devices are built along with manual routing and placement. In semi-custom transistors (pMOS, nMOS) are inbuilt, but in fully custom transistors (pMOS, nMOS) are not inbuilt. In this approach designer designs own transistors, gates, modules and circuits by follow the lambda design rule. In this approach performance of a chip is maximizes in terms of area and power. Fig.11. represent the fully custom layout. This layout is checked for DRC if there is no error then it is simulated, and timing diagram of fully custom layout is generated. Timing diagram consist many waveforms which is verified by comparing the circuit operation. Fig.12. shows the timing diagram of automatic generated layout. The layout area, number of pMOS, nMOS used in the circuit is measured from the properties.

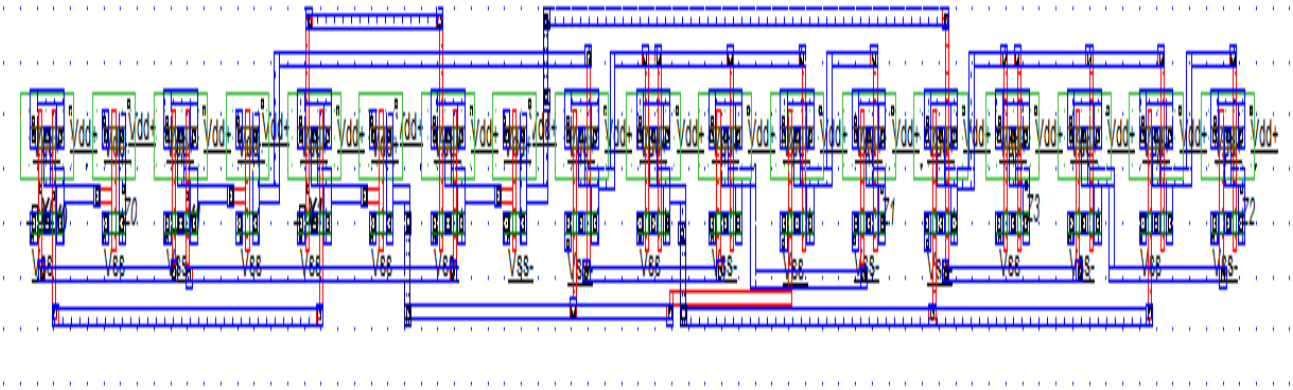

Fig. 11. Two bit multiplier Fully-Custom layout

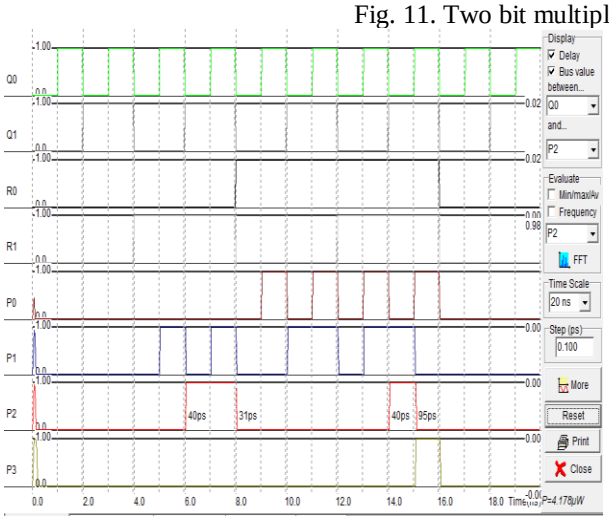

Fig. 12. Timing Diagram of fully-custom layout

We measure the consuming power 4.178 µwatt by this layout simulation, and the layout area is measured from the properties. Area required for this particular layout is 109.0 µm². Width is 37.0 µm and height is 3.0 µm. From the electrical properties we note that 91 electrical nodes are used, 32 pMOS devices are used and 30 nMOS devices are used. Fully custom design is better from semi-custom design and fully automatic design because in this manual active device are built along with manual routing and placement.

5. RESULT COMPARISION

The performance of two bit binary multiplier is compared on the basis of fully automatic, semi-custom and fully-custom based approaches. The performance parameters are area and power. From the above results which are discussed in paper comparative study can be done between fully automatic, semi-custom and fully-automatic designing approaches when the input applied to two bit binary multiplier is same in all three approaches in term of rise time, fall time, high time, low time etc. In fully automatic, semi-custom and fully custom approach for all the inputs high level is 1.00 volt, low level is 0.00 volt, rise time is 0.010 ns, fall time is 0.10 ns but time low and time high is different. For input Q_0 time low and time high is 0.990 ns. For input Q_1 time low and time high is 1.990 ns. For input R_0 time low and time high is 7.990 ns. For input R_1 time low and time high is 3.990 ns. Second thing is why the area of semi-custom and fully custom is reduced. Area is reduced because in fully automatic layout is generated automatic when we compile Verilog file. In semi-custom we take transistor from the software then make module gates etc., and in fully custom we make module, gates as well as transistor. The comparison of gates, devices and transistor which are used in circuit is compare in term of area shows in Table 2. Table 3 shows the comparative analysis of

two bit binary multiplier in fully automatic, semi-custom and fully custom approach in terms of both area and power.

Table 2. Comparative Analysis of Area for devices

Device	Semi-custom	Fully-custom
pMOS	1.3µm²	1.0 µm²
nMOS	0.5 µm²	0.4 µm²
2 pMOS	1.8µm²	1.3µm²
2 nMOS	0.9µm²	0.5µm²
And gate	7.0 µm²	5.2 µm²
Nand gate	3.4 µm²	2.4 µm²
Half adder	30.6 µm²	24.5 µm²

Table 3. Comparative Analysis of Area and power

Approach	Area (µm²)	Power (µw)
Fully automatic	181.1	8.398
Semi-custom	134.7	7.815
Fully-custom	109.0	4.178

Comparative analysis table shows that the performance of all three layout approach. In terms of both area and power the fully custom layout approach gives the better performance as compare to other layout design approach. Fig.13. shows the comparative analysis of two bit binary multiplier in fully automatic, semi-custom and fully custom approach in terms of both area and power in the form of bar graph.

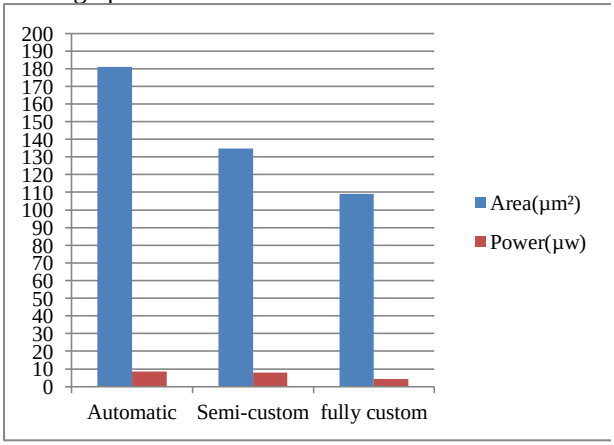

Fig. 13. Area and Power graph

From the graph shown in Fig. 13 and Table 3 which is shown above is clear that the fully custom approach is better in terms of both area and power. From the above results and discussion clearly shown fully-custom is 19.07 % better than semi-custom and 39.81 % better than fully automatic approach in terms of area. In terms of power fully-custom is 52.24 % better than fully automatic and 46.53 % better than semi-custom approach.

6. CONCLUSION

Efficient two bit binary multiplier is implemented with microwind software in VLSI using 90nm CMOS technology. For efficient design make half adder and AND gates which take less area and consume less power. From the above result which is discussed in the paper it is clear that the fully-custom layout is more efficient in term of both area and power. Fully automatic design takes 181.1 µm² area and 8.748 µw power. Semi-custom design takes 134.7 µm² area and 7.815 µw power. In semi-custom design the area reduced 46.4 µm² and power reduced 0.933 µw. In semi-custom design the area and power both reduced so semi-custom design is better from fully automatic design in term of both power as well as area. Fully-custom design takes 109.0 µm² area and 4.178 µw power. In fully-custom design the area reduced 72.1 µm² and power reduced 4.57 µw when compare with fully automatic design. In fully-custom design the area reduced 25.7 µm² and power reduced 3.637 µw when compare with semi-custom design. In fully-custom design the area and power both reduced as compare to fully automatic and semi-custom so fully-custom design is better from fully automatic design and semi-custom design in term of both power as well as area.

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