International Journal of Research in Advent Technology, Vol.7, No.4, April 2019
E-ISSN: 2321-9637
Available online at www.ijrat.org

Comparative Study of Carbon Nanotube Based Thin Film Transistors on Flexible Substrates

M. C. Chandrashekhar[1], K. C. Narasimhamurthy[2]
Associate Professor[1], Professor[2], Department of E and C[1] , Department of TCE[2], Sri Siddhartha Institute of Technology[1], Siddaganga Institute of Technology[2]
Email: mccshekhar@gmail.com[1], kcnmurthy@gmail.com[2]

Abstract- A review of fabricated carbon nanotube based thin film transistors (CNTTFTs) on different substrate materials and the fabrication techniques for thin film transistors on flexible substrates are presented. The performance parameters of CNTTFTs reported by different groups are also presented. The CNTTFTs exhibited the extreme bendability without much change in the electrical performance. The fabricated single walled carbon nanotube based thin film transistors (SW CNTTFTs) on flexible substrates are compared based on their on/off current ratio and mobility are also discussed.

Index Terms- CNTTFTs, SW CNTTFTs, flexible, On/Off current ratio, mobility, substrates, bendability.

1. INTRODUCTION

The revolutionary advances have been taken place in VLSI industry in the field of materials and devices. The new materials are replacing silicon in the field of flexible electronics. The flexible electronics uses thin film transistors (TFTs). The performance limitations of organic thin film transistors (OTTFTs) are low charge carrier density and processing related difficulties due to their insoluble nature under ambient conditions [1, 2, 3, 4]. Thin film transistors using amorphous silicon have disadvantages like high temperature process and reduced electron mobility. Lesser mobility reduces the operation frequency of the device to few KHz and the device cannot be used for high frequency. The carbon nano tubes (CNTs) are the new materials which are used in the field of flexible electronics. The CNTs are small graphite sheets rolled into a seamless cylinder. Nano tubes can be of two types, single walled and multi walled. Single walled carbon nanotubes (SWCNTs) consist of a single layer whereas multi-walled nanotubes consist of several cylindrical concentric layers wrapped around each other. The diameter and its helicity decide whether nano tubes are metallic or semiconducting. The diameter of the tube also decides the energy band gap of the carbon nano tube. Carbon nanotubes have largest strength to weight ratios of any material. The thin film transistors using single walled carbon nanotubes as the channel material are preferred because of their excellent electrical and mechanical properties. The field effect mobility of 79000 cm^2 /Vs was reported in the FETs based on individual CNTs [5]. However the mobility of TFT using SWCNTs is less due to the multiple CNT–CNT contacts in the networks. The mobility in CNT TFTs is in the order 10-100cm^2/Vs [6]. CNT based flexible FETs are capable of achieving high speed operation compared organic TFTs [7, 8, 9]. The performance parameters such as on current, on/off current ratio, transconductance g_m of TFTs depend on the density of SWCNTs. The film of SWCNTs on non-treated surface has low density of SWCNTs. In order to improve the performance of TFTs and to increase the density of SWCNTs [10, 11] surfaces are treated with adhesives. Single-walled carbon nanotubes are deposited on the Si surface to increase the nanotube density. TFTs with sorted semiconducting SWCNTs of different purity are fabricated [4, 12, 13, 14, 15]. The SWCNTs thin film is deposited on a modified Si/SiO_2 surface.

SWCNTs based flexible thin film transistors fabrication techniques, transistor performance on different flexible substrates are compared. The carbon nanotube thin film transistors (CNTTFTs) on flexible substrates are more widely used in stretchable, flexible electronics like E-textiles, finger print scanners, X-ray imaging, light weight display, photovoltaic, electronic tags, solid state lighting, and intelligent smart cards. The review of flexible TFTs is based on substrate materials, fabrication techniques, transistor performance is done.

2. FABRICATION TECHNIQUES FOR THIN FILM TRANSISTORS ON FLEXIBLE SUBSTRATES

The fabrication of single walled carbon nanotube based thin film transistors (SW CNTTFTs) on flexible substrates can be categorized into three types i.e. solid phase, liquid phase and gas phase fabrications [16-23] based on the formation of the SWCNTs thin films on the flexible substrates.

2.1. Solid phase fabrication

The SWCNTs are deposited on a solid or rigid wafer and transferred on to a flexible substrate. Prior to the SWCNTs transfer, flexible substrate was pre-patterned with gate electrodes followed by source and drain electrodes. Fig. 1(a) - (e) shows the fabrication of fully transparent aligned SWCNT transistors. In [17] Nanotubes were first grown on quartz substrates and then transferred to prepatterned glass or polyethylene

terephthalate (PET) substrates. The PET substrate was prepatterned with indium tin oxide (ITO) gate electrodes, followed by patterning of transparent source and drain electrodes. Device dimensions are limited by the size of the rigid surface.

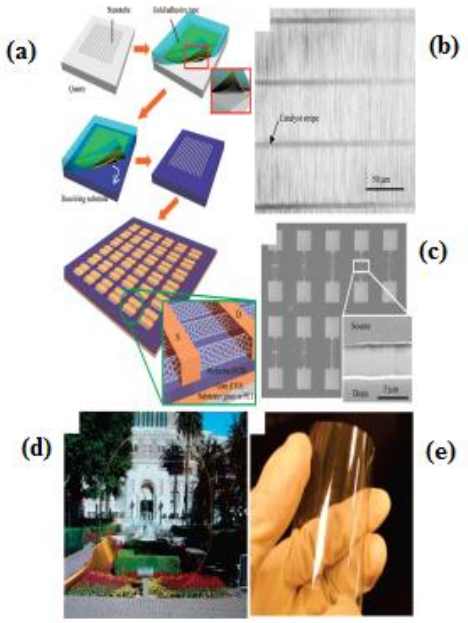

Fig.1. Fabrication of fully transparent aligned SWCNT transistors [17] : (a) Schematic diagram of aligned SWCNT transfer and a device structure consisting of a substrate (glass or PET), ITO as back gate, SU8 as dielectric, aligned SWCNTs as channel, and ITO as source and drain. (b) Scanning electron microscopy (SEM)image of transferred aligned SWCNTs on SU8 on a glass substrate. (c) SEM image of devices showing the ITO source and drain electrodes fabricated on glass. Inset: SEM image of aligned nanotubes bridging ITO electrodes. (d) Optical micrograph of fully transparent aligned SWCNT transistors on a 4 inch glass wafer. (e) Optical micrograph of fully transparent aligned SWCNT transistors on a PET sheet of 3 inch x 4 inch.

In [18] the chemical vapor deposition (CVD) method was used to synthesize CNT thin film on silicon dioxide-silicon wafers. Using optically soft lithography technique the SWCNT thin film is etched into strips. The source and drain electrodes and the isolation of each device were patterned using standard photolithography, electron beam evaporation, gold wet chemical etching and oxygen plasma etching. The predefined source and drain electrodes and SWCNT networks on the growth wafers for transfer to a polyimide substrate coated with liquid polyurethane were encapsulated using polyamic acid. The curing of the liquid polyurethane and polyamic acid

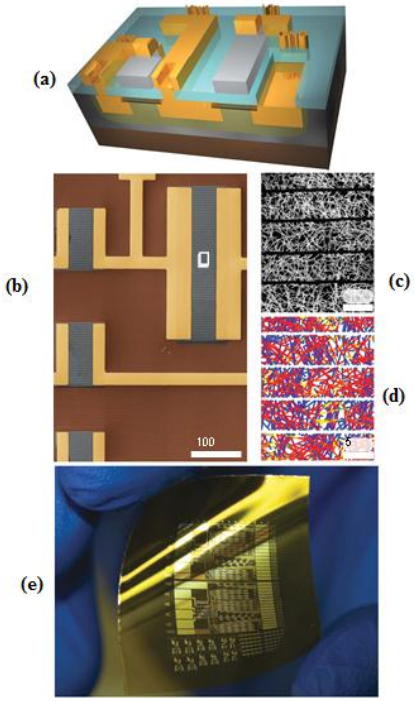

Fig.2. Illustration, scanning electron microscope images, theoretical modeling results and photographs of flexible SWCNT integrated circuits on plastic [18] : (a) Cross-sectional diagram of a SWCNT P-metal oxide semiconductor (PMOS) inverter on a PI substrate. (b) Scanning electron microscope image of part of the SWCNT circuit, made before deposition of the gate dielectric, gate or gate-level interconnects. The source–drain electrodes (gold) and substrates (brown) had been colorized to highlight the SWCNT network strips (black and grey) that form the semiconductor. (c) Magnified view of the network strips corresponding to a region of the device channel highlighted with the white box in b. (d) Theoretical modeling results for the normalized current distribution in the on-state of the device (view as in c), where color indicates current density (yellow, high; red, medium; blue, low). (e) Photograph of a collection of SWCNT transistors and circuits on a thin sheet of plastic (PI).

completes the transfer process subsequently. After deposition of high capacitance dielectric layer of hafnium dioxide the metal gate was formed. Vias and windows were provided for probing by wet etching through patterned photoresist and the metal inter connection were carried out and then four bit decoder was designed. The explained process is given in the Fig. 2 (a) - (e).

The floating catalyst (aerosol)-chemical vapor deposition (FC-CVD) techniques were used to continuously grow carbon nanotubes [19] in atmospheric pressure by feeding a carbon source gas with a catalyst precursor. At room temperature nanotubes are collected on a membrane filter for short time between 1 and 5 sec. The filter was dissolved in acetone, and as-grown nanotubes are transferred from

the filter to the substrate on which the TFT electrodes are prepared. The nanotubes located outside the channel areas are removed by oxygen plasma treatment. The explained process is given in the Fig. 3(a) - (e).

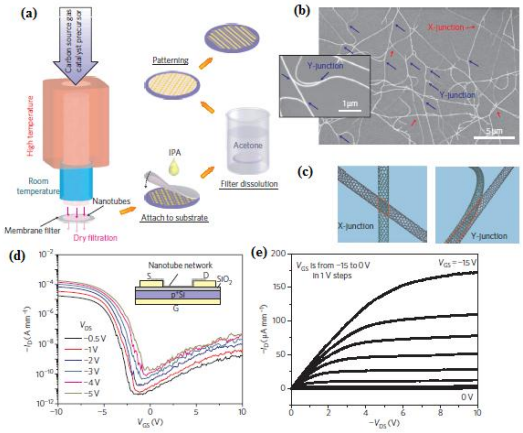

Fig.3. Carbon nanotube growth and device fabrication [19]:(a) Schematic of carbon nanotube growth, collection by filter, transfer and patterning.(b) SEM image of carbon nanotube film transferred onto a Si/SiO_2 substrate. Carbon nanotube collection time, 2 s. Inset: magnified view of Y-junctions. The red and blue arrows indicate X- and Y-junctions, respectively. (c) Schematics of X- and Y-junctions. (d) Transfer (I_D V/S V_{GS}) Characteristics at various drain to source voltage (V_{DS}) values ranging from 20.5 to 25 V. Channel length (L)= width (W) =100 µm. Inset: schematics of the bottom-gate carbon nanotube TFT on a silicon(Si) /SiO_2 substrate. (e) Output (drain current (I_D) V/S V_{DS}) characteristics of the same device exhibiting saturation behavior.

2.2 Liquid Phase Fabrication

SWCNT solution is prepared and deposited on a flexible substrate by spin coating, dip-coating [20], ink jet printing [21, 22] /gravure printing, spray coating [23, 24] etc. to form a thin film. Subsequent processes of patterning of gate electrodes, source and drain electrodes are carried out.

In the dip-coating process and fabrication [20] the optical lithography was used to define the micro channel on silicon substrate, modified parylene-c as adhesive layer. The silicon substrate with parylene-c was dipped into aqueous SWCNT solution which was terminated with carboxylic acid group and pulled up slowly. The SWCNTs adhering to the surface of the parylene-c formed stripe structure as shown in [20]. Peel-off the flexible parylene-c SWCNT film from the substrate. sub-sections and sub-subsections are numbered in Italic. Use double spacing before all section headings and single spacing after section headings.

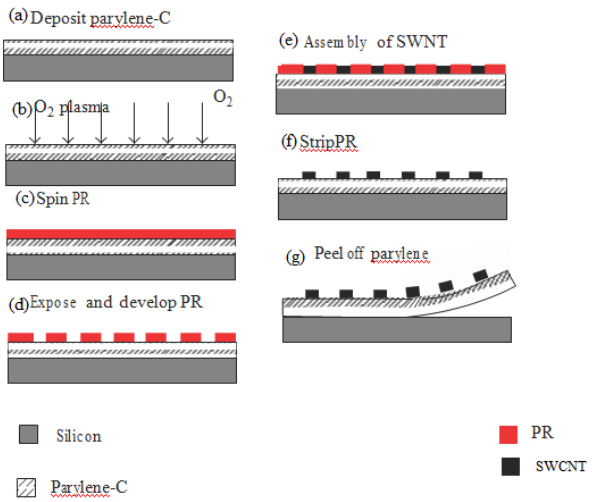

Fig.4. Schematic drawing of the patterning of SWCNTs onto a flexible substrate using dip-coating [20].

The Fig. 4(a) - (g) show the process flow diagram of the direct patterning of SWCNTs on to a flexible substrate. The parylene–c film hydrophobic surface was changed to hydrophilic by disposing the parylene film by O_2 Plasma for 30 sec. and the micro channel was defined by optical lithography. The chip was dipped into aqueous SWCNT solution and pulled it up slowly with a speed of 0.1mm/min. Photo resist was removed by acetone after completing dip- coating.

High mobility carbon nano tube thin film transistors were fabricated on a polymeric substrate by E.S.Snow et al. [25].The devices fabricated, exhibited field effect mobility of 1500 cm^2/Vs and normalized transconductance of 0.5 ms /mm. The ratio of on-current to off-current achieved was 100. Layer of polyimide of 10 µm thickness was spin coated on to a silicon wafer and cured in nitrogen ambient in stages of 100^oC steps for 1 hour each to a maximum temperature of 300^oC Electron beam deposition and lift-off was used to form metal fingers and contact pads on the polyimide surface of 25 nm thickness. Electron beam evaporation and lift-off of fused silica was used to cover gate metal fingers with 100 nm-thick gate dielectric pads of silicon oxide. The wafer was soaked for one hour in a solution of 3-aminopropyl triethoxysilane. The wafer was blown dry and then soaked in a prepared solution of SWCNTs. The wafer was removed from the SWCNTs solution and blown dry when a continuous nanotube network has formed. The entire wafer was coated with the SWCNTs network. The residual sodium dodecyl sulphate (SDS) was removed by soaking the wafer in de-ionized (DI) water for at least one hour. The 100 nm of Titanium source–drain contact pads were formed by electron beam evaporation and lift-off. The removal of the unwanted SWCNTs was done by protecting the active area of the devices by the patterns of the photoresist and then commercial snow jet from Applied Surface Technologies was used. Fig.5 shows an optical image of an array of SWCNT TFTs on a polyimide substrate. The lower inset shows

the same film supported by a glass substrate. The upper inset is a magnified image of an individual TFT.

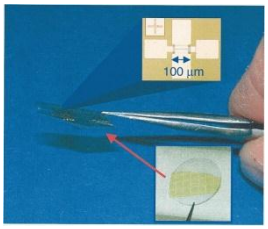

Fig.5. An optical image of fabricated SW CNTTFTs on a polyimide film of thickness 10 µm [25].

The demonstration of fully printed, top gated TFTs was done [26, 27, 28]. The 99% semiconductor purity nanotubes were used. The scalable inverse gravure printing process [27] was used printing registration accuracy of ±10 µm. source, drain and gate silver metal electrodes were processed using multi step printing and also inorganic/organic high–k gate dielectric on PET substrate. The devices exhibits hole mobility of up to 9 cm^2/Vs and on/off current ratio of 10^5. Fig.6 (a) shows the processing steps for fabricating fully printed SW CNTTFTs on a PET substrate. Fig. 6(b) shows the Scanning Electron Microscope of a SWCNT network deposited on a PET substrate.

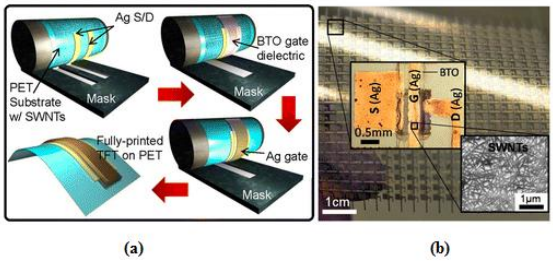

Fig. 6. Printing process [27]: (a) Schematic diagram showing the printing process scheme. (b) SEM image of a SWCNT network deposited on a PET substrate.

This method has reduced energy consumption during manufacturing, reduced cost of production. It can be used for mass production.

2.3 Gas Phase Fabrication

The CNT thin film is directly transferred on to the substrate after it is formed in a gas-phase [29, 30] environment. The contamination occurs in liquid phase or in solid phase fabrication in transferring process. The dry process of fabrication of CNTFTs [30] was demonstrated by M.Y Zavodchikova et al. The fabrication of CNTTFTs on flexible substrates was done by directly transferring CNT thin films which were synthesized by floating catalyst method on to the substrate. The fabrication of high performance TFTs and integrated circuits on flexible and transparent substrates using floating catalyst CVD followed by simple gas phase filtration and transfer process [29]. The unique morphology of CNT network was reported when compared to CNTs prepared by solution based technique.

3. COMPARATIVE STUDY OF CARBON NANOTUBE BASED THIN FILM TRANSISTORS ON FLEXIBLE SUBSTRATES

The comparison of CNTFTs on flexible substrates were done on based on the performance parameters like on-current, on/off current ratio, mobility, trans conductance and type of the oxide, purity of SWCNTs. The table 1 gives the comparison based on the flexible substrates used, device dimensions, purity of SWCNTs, gate oxide used, on/off current ratio, mobility, contact metal used, transconductance of the 13 CNTTFTs fabricated by different groups.

NR – Not reported, PI - Polyimide, PET - Polyethylene terephthalate, PEN - Polyethylene naphthalate, PU - Polyurethane, PMMA - Poly methyl methacrylate

Table 1.Comparison of TFTs implemented on flexible substrates.

Sl. No.	Flexible substrate used	Width/ Length (μm/ μm)	Purity of CNTs (%)	Gate oxide used	On/off current ratio	Mobility (cm^2/Vs)	Contact metal used	Trans conductance g_m	References
1.	PI	130/7	NR	SiO_2	100	150	Ti	0.5 mS/mm	[25]
2.	PI, PU	5/100	NR	HfO_2	$>10^5$	80	Gold	0.12 μS /μm	[32]
3.	PET	200/50	95	Epoxy and SiO_2	10^2	2	Graphene films on Ni	NR	[40]
4.	PEN	10/55	NR	Al_2O_3	10^5	5	Au	NR	[41]
5.	PEN	100/100	NR	PMMA	$1.5X10^5$	1027	carbon	NR	[31]
6.	PI	NR	95	Al_2O_3	10^5	10-35	Ti over Au	NR	[42]
7.	PET	NR	80-90%	Al_2O_3/ PMMA bilayer	10^3	1-33	CNTs	NR	[33]
8.	PEN	130/115	NR	PI	10^4	157	Inks of silver nano particles	NR	[31]
9.	PET	NR	NR	NR	$4X10^3$	1.5	Copper over silver	NR	[43]
10.	PET	1250/8.5	99	Inorganic /organic high k=17	10^5	9	Ag	3.35 μS/nm	[27]
11.	PI	200/100	NR	NR	10^4	60	Pd	NR	[44]
12.	NR	3/8	99	NR	$2X10^3$	40.7	NR	NR	[45]

The flexible substrates like Polyimide (PI), PET, Polyethylene naphthalate (PEN) were used. The gate oxides like silicon dioxide (SiO_2), hafnium dioxide (HfO_2), aluminium trioxide (Al_2O_3), Al_2O_3/Poly methyl methacrylate (PMMA) bilayer, inorganic/organic high-k=17 materials were used. The SWCNTs of 95%, 98%, 99% semiconducting purity were used. The contact metals like Ti, gold, graphene films on nickel, Ti over Au, Ti over Pd, copper over silver, silver were used for source and drain contacts.
The high mobility of 157 cm^2 / Vs was achieved [31] with on/off current ratio of 104 from the fabrication of bottom gate CNTTFT with channel length and channel width of 115 μm and 130 μm respectively on PEN film using flexographic printing process. PMMA of 4.1 μm thickness was used as gate oxide. The source and drain electrodes were formed by Ag nano particle ink.
The high on/off current ratio of $6x10^6$ was achieved [19] with mobility of 35 cm^2 / Vs from the fabrication of bottom gate CNTTFT with channel length and channel width of 100 μm. The substrate used was PEN. The gate formed was bottom gate. The SiO_2 was used as a gate dielectric. For source and drain, Ti/Au metal electrodes were used and fabricated using standard photolithography, electron-beam evaporation and lift-off processes.

Mechanical flexibility of the devices on PET substrate was tested by bending down the substrate to different radii along the channel length and electrically measured. The noticeable degradation of electrical performance was not observed when severely bent in TFTs operation. The results of the bending tests done on the fabricated CNTTFTs on the flexible substrates are compared and are listed in table 2. SWCNTs used as channel can be bent and there is a small change in the electrical performance of the devices [17,27,30,32,33,34,35,36,37,38,39].

In the work [40] the graphenes were used as electrodes, only small changes in μ/μ_0 is observed for the range of strains up to 2.2%. The thing observed from the work [35] the limit for bending is the practical bendability. CNTTFTs on flexible substrates are limited by oxides, source and drain, gate electrodes and the mechanical properties of the flexible substrates.

Table 2: Comparison of the bending tests done on the CNTTFTs fabricated on the flexible substrates.

Sl.No.	Substrate	W/L (µm/ µm)	SWCNTs Purity (%)	Variation upon bent	Bent radius (mm)	I_{ON}/I_{OFF} (µA/ µA)	μ_{carr} (cm^2/Vs)	References
1.	PI	300/100	99%	No much change	NR	20	NR	[34]
2.	PES	NR	HiPCo	No much change	NR	$>10^2$	150	[35]
3.	PET	100/30	NR	No much change	NR	3×10^4	1300	[17]
4.	PI	5/50	NR	No much change	5	10^5	80	[32]
5.	PC	NR	NR	No much change	1.5	10^3	55	[36]
6.	PET	200/25	95%	Deformation	4.25	10^2	2	[40]
7.	PET	100/10	NR	No much change	NR	10^3	1-33	[33]
8.	PET	125/85	99%	No much change	1	10^5	9	[27]
9.	PET	1000/1005	100	No much change	NR	10^5	7	[38]
10.	PET	100/100	NR	No much change	7.8	10^5	1027	[30]

NR - Not reported, PC - Parylene C, PES - Polyether sulphone, HiPCo - Hi pressure carbon monoxide

4. CONCLUSION

We have reviewed the carbon nano tube based TFTs on different substrates. The disadvantages of organic thin film transistors and amorphous silicon thin film transistors have been discussed. The fabrication techniques for carbon nanotube thin film transistors on flexible substrates were also reviewed. The performance comparison of fabricated carbon nano tube based thin film transistors on flexible substrates was discussed. The CNTTFTs fabricated on flexible substrates exhibits good electrical performance with the extreme bendability of the substrate. The low cost and temperature, fabrication methods for the mass production of high performance CNTTFTs on flexible substrates are the areas in which the researchers have to concentrate. The repeatable characteristics of flexible CNTTFTs are desired, to use these fabricated devices in high-performance flexible electronics applications.

REFERENCES

[1] H.Klauk,M .Halik,U. Zscieschang, F.Eder, D.Rande, G.Schmid, C.Dhehm, "Flexible organic complementary circuits", IEEE Trans.Electron Devices, vol.52, No.4, pp.618-622, Apr.2005.

[2] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," IBM Journal of Research and Development, Vol.45, pp.11-27, Jan. 2001.

[3] Stephen R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," Nature, vol. 428, pp.911-918, Apr.2001.

[4] K.C.Narasimhamurthy, and Roy Paily, "Performance comparison of interdigitated thin-film-field effect transistors using different purity semiconducting carbon nanotubes," Advanced materials research, Vol. 181-182, pp.343-348, Jan. 2011.

[5] T.Durkop, S.A.Getty, E.Cobas, and M.S.Fuhrer, "Extra ordinary mobility in semiconducting nano tubes", Nano Lett., vol.4, No.1, pp.35-39, Jan.2004.

[6] Satish Kumar, Baratunde A. Cola, Roderick Jackson, Samuel Graham "A Review of Carbon Nanotube Ensembles as Flexible Electronics and Advanced Packaging Materials" Journal of Electronic Packaging, Vol. 133, pp. 020906-1, June 2011.

[7] S.Rosenblatt, H. Lin, V.Sazonova,S. Tiwari, and P.L.Mc Even, "Mixing at 50 GHz using a single-walled carbon nanotube transistor", Appl.Phys.Lett., vol.87, No.15, pp.153111, Aug.2005.

[8] A.A.Pesetski, J. E. Baumgardner, E.Folk, J.X.Przybysz, J.D.Adam, and H.Zhang, "Carbon nanotube field effect transistor operation at microwave operation", Applied physics lett., vol. 88, No.11, pp. 113103, Mar.2006.

[9] S.Li,Z.Yu,S.Yen, W.C.Tang, and P.J.Burke, "Carbon nanotube transistor operation at 2.6 GHz", Nano lett., vol.4., No.4, pp.753-756, Mar.2004.

[10] Lay, M.D., Novak, J.P., Snow, E.S.: 'Simple route to large-scale ordered arrays of liquid-deposited carbon nanotubes', Nano Lett., vol.4, No.4, pp. 603–606, Mar.2004.

[11] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, "Self-sorted, aligned nanotube networks for thin-film transistors," Science, vol. 321, No.5885, pp.101-104, Jul.2008.

[12] L. Hu, D. S. Hecht, and G. Gruener, "Percolation in transparent and conducting carbon nanotube networks," Nano Lett., vol. 4, No.12, pp.2513-2517, Oct. 2004.

[13] E. S. Snow, J. P. Novak, P. M. Campbell, and D. Park, "Random networks of carbon nanotubes as an electronic material," Appl. Phys. Lett, vol. 82, No.13, pp. 2145, Mar. 2003.

[14] M. Engel, J. P., Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, and P. Avouris, "Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays," ACS Nano, vol. 2, No.12, Dec. 2008, pp. 2445-2452.

[15] C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. G. D. Arco, and C. Zhou, "Wafer-scale fabrication of separated carbon nanotube thin-film transistors for display applications," Nano Lett., Vol. 9, No.12, pp. 4285-4291, Nov. 2009.

[16] Dong-Ming Sun, Chang Liu,Wen-CaiRen, and Hui-Ming Cheng, "A review of carbon nanotube-and graphene-based flexible thin film transistors," Small, vol. 9, No.8, pp.1188-1205, Mar. 2013.

[17] Fumiaki N. Ishikawa, Hsiao-kang Chang, Koungmin Ryu, Po-chiang Chen, Alexander Badmaev, Lewis Gomez De Arco, Guozhen Shen, and Chongwu Zhou "Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrates," ACS Nano, vol. 3,No.1, pp.73–79 , Dec. 2008.

[18] Q.Cao, H.Kim, N.Pimparkar, J.P.Kulkarni, C.Wang, M.Shim, K. Roy, M.A. Alam, and J.A .Rogers, "Medium-scale carbon nanotube thin film integrated circuits on flexible plastic substrates," Nature,Vol.454, pp.495-500, Jul. 2008.

[19] Dong-ming. sun, MarinaY. Timmermans, YingTian, Albert G. Nasibulin, Eskoi. kauppinen, Shigeru Kishimoto, Takashi Mizutani and Yutaka Ohmo, "Flexible high -performance carbon nanotube integrated circuits" Nature Nanotechnology vol.6, No.3, pp.156-161, Mar.2011.

[20] X. Xiong, C-L. Chen, P. Ryan, A.A. Busnaina, Y. J. Jung, and M.R. Dokmeci, "Directed assembly of high density single walled carbon nanotube patterns on flexible polymer substrates", Nano technology, vol. 20, No. 29, pp. 295302, Jul. 2009.

[21] HaruyaOkimoto, TaishiTakenobu, KazuhiroYanagi , YasumitsuMiyata, Hidekazu Shimotani , Hiromichi Kataura ,and Yoshihiro Iwasa "Tunable carbon nanotube thin film transistors produced exclusively via inkjet printing," Advanced materials, vol.22,No.36, pp.3981-3986, Sept.2010.

[22] M.Ha,Y. Xia, and A AGreen et al., "Printed, sub-3V digital circuits on plastic from aqueous carbon nano tube inks," ACS Nano, Vol. 4, No.8, pp.4338-4395, Jun. 2010.

[23] E.Artukovic, M. Kaempgen, D.S.Hecht, S.Roth, and G.Gruner, "Transparent and flexible carbon nanotube transistors," Nano Letters, vol.5, No.4, pp.757-760, Mar.2005.

[24] Z. Li, H.R. Kandel and E. Dervishi et al., "Does the wall number of carbon nanotubes matter as conductive transparent material?," Applied Physics Letters, vol.91, No.5, pp.053115, Aug. 2007.

[25] E.S.Snow, P.M.Campbell, M.G.Ancona, and J.PNovak, "High-mobility carbon-nanotube thin film transistors on a polymeric substrate," Applied Physics Letters, vol.86, No.6, pp.033105, Jan. 2005.

[26] Jianwen Zhao,Yulong Gao,Weibing Gu, Chao Wang, Jian Lin, Zheng Chen and Zheng Cui, "Fabrication and electrical properties of all-printed carbon nanotube thin film transistors on flexible substrates," Journal of Materials Chemistry, vol.22, No.38, pp.20747-20753, Aug.2012.

[27] Pak Heng Lau, Kuniharu Takei, Chuan Wang, Yeonkyeong Ju, Junseok Kim, Zhibin Yu, Toshitake Takahashi, Gyoujin Cho, and Ali Javey, "Fully printed, high performance carbon nanotube thin-film transistors on flexible substrates," Nano letters,vol.13, No.8, pp.3864-3869, Jul.2013.

[28] J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian, and G. Cho, "Fully gravure-printed D-flip-flop on plastic foils using single-walled carbon-nanotube-based TFTs," IEEE Electron Device Letters, vol. 32, No.5, pp. 638-640, May 2011.

[29] M.Y.Zavodchikova, T.Kulmala, A.G.Nasibulin, V.Ermolov, S.Fransila, K.Grigoras, and E.I.Kauppinen, "Carbon nano tube thin film transistors based on aerosol methods," Nanotechnology, vol. 20, No.8, pp.085201, Feb. 2009.

[30] Dong-Ming Sun, Marinav Y. Timmermans, Anti kaskela,Albert G.Nasibulin,Shigeru Kishimoto, Takashi Mizutani and Yutaka Ohmo "Mouldable all-carbon integrated circuits," Nature communications, vol. 4, pp.2302, Aug. 2013.

[31] V.Yutaka Ohno Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan,. Active-Matrix Flat panel Displays and Devices (AM-FPD), 2013 Twentieth International Workshop on date 2-5 July 2013.

[32] Q. Cao, H. S. Kim, N. Pimparkar, J. P. Kulkarni, C. J. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers, "Medium-scale carbon nanotube thin- film integrated

circuits on flexible plastic substrates," Nature, vol.454, No.7203, pp.495-500, Jul.2008.

[33] V.K Sangwan, A. Southard, T.L Moore, V.W. Ballarotto, D.R Hines, M.S.Fuhrer, and E.D.Williams "Transfer printing approach to all-carbon Nanoelectronics," Microelectronic Engineering,vol.88, No.10, pp.3150-3154, Oct.2011.

[34] Daniel Pham, Harish Subbaraman, Maggie Yihong Chen, Xiaochuan Xu, and Ray T. Chen "Bending tests of carbon nanotube thin-film transistors on flexible," Article in Proc. SPIE 7761, Aug. 2010. DOI: 10.1117/12.864066.

[35] Tae-Geun Kim, Jongseung Hwang, Jeongmin Kang, Sangsig Kim, and Sung Woo Hwang, "Fabrication of nano meter-scale carbon nanotube field-effect transistors on flexible and transparent substrate," Journal of Nano science and Nanotechnology, vol. 11,No. 2, pp.1393–1396, Feb.2011.

[36] Selvapraba Selvarasah, Kyle Anstey, Sivasubramanian Somu, Ahmed Busnaina, and Mehmet R. Dokmeci1, "Highly flexible and biocompatible carbon nanotube thin film transistors," 9th IEEE Conference on Nanotechnology, 26-30 Jul. 2009, Genoa, Italy, pp.29-32.

[37] Seung-Hyun Hur, O Ok Park and John. A. Rogers, "Extreme bendability of single-walled carbon nanotube networks transferred from high-temperature growth substrates to plastic and their use in thin-film transistors," Appl. Phys. Lett. vol.86, No.24, pp.243502 -243505, Jun. 2005.

[38] Xuan Cao, Haitian Chen, Xiaofei Gu, Bilu Liu, Wenli Wang, Yu Cao, Fanqi Wu, and Chongwu Zhou, "Screen printing as a scalable and low-cost approach for rigid and flexible thin-film transistors using separated carbon nanotubes," ACS Nano, Vol.8, No.12, pp.12769–12776. Dec.2014.

[39] Chuan Wang, Jun-Chau Chien, Kuniharu Takei, Toshitake Takahashi, Junghyo Nah, Ali M. Niknejad, and Ali Javey, "Extremely bendable, high-performance integrated circuits using semiconducting carbon nanotube networks for digital, analog, and radio-frequency applications," Nano Letters,vol.12, No.3, pp.1527-1533,Feb. 2012.

[40] Sukjae Jang, Houk Jang, Youngbin Lee, Daewoo Suh, Seunghyun Baik, Byung Hee Hong and Jong-Hyun Ahn, "Flexible transparent single -walled carbon nanotube transistors with graphene electrodes" Nano technology ,vol.21, pp. 425201-425206,2010.

[41] Marina Y Timmermans, Kestutis Grigoras, Albert G Nasibulin,Ville Hurskainen, Sami Franssila, Vladimir Ermolov and Esko I Kauppinen,"Lithography-free fabrication of carbon nanotube network transistors," Nano technology, Vol. 22, pp.065303-065309, Jan.2011.

[42] Bhupesh Chandra, Hong Sik Park, Ahmed Maarouf ,Glenn J. Martyna, and George S. Tulevski, "Carbon nanotube thin film transistors on flexible substrates," Applied Physics Letters,vol.99, No.7, pp.072110-072113, Aug. 2011.

[43] Jianwen Zhao,Yulong Gao,Weibing Gu, Chao Wang, Jian Lin, Zheng Chen and Zheng Cui, "Fabrication and electrical properties of all-printed carbon nanotube thin film transistors on flexible substrates," Journal of Materials Chemistry, vol.22,No.38, pp.20747-20753, Aug.2012.

[44] Pingqi Gao and Qing Zhang "Encapsulate-and-peel: fabricating carbon nanotube CMOS integrated circuits in a flexible ultra-thin plastic film," Nano technology, vol.25, No.6, pp.065301-065308, Feb.2014.

[45] Alireza Mousavi, Patrizia Lamberti, Vincenzo Tucci, Veit Wagner "Feasible Industrial Fabrication of Thin Film Transistor based on Randomized Network of Single Walled Carbon Nanotubes", ASMC 2013, 14-16 May 2013, DOI: 10.1109/ASMC.2013.

M. C. Chandrashekhar received the B.E. degree in Electronics and Communication Engineering from Bangalore University, Bangalore, India and the M.E. degree in Digital Electronics from Karnatak University, Dharwad, India in 1997. Currently, he is an Associate Professor with the Department of Electronics and Communication Engineering, Sri Siddhartha Institute of Technology, Tumakuru and working toward the Ph.D. degree with the Department of Telecommunication Engineering, Siddaganga Institute of Technology, Visvesvaraya Technological University, Tumakuru, India. His research interests include the design and fabrication of digital circuits using carbon nanotube thin film transistors on flexible substrates.
e-mail:mccshekhar@gmail.com
(Corresponding Author)

K. C. Narasimhamurthy received the B.E. degree in Electronics and Communication Engineering from Bangalore University, Bangalore, India and the M.Tech. degree in Industrial Electronics from Mysore University, Mysore, India in 1995 and the Ph.D. degree in VLSI from the Indian Institute of Technology, Guwahati, India in 2011. Currently, he is a Professor with the Department of Telecommunication Engineering, Siddaganga Institute of Technology, Tumakuru, India. His research interests include the design of analog circuits using carbon-nanotube transistors, design, and fabrication of digital circuits using carbon nanotube thin film transistors on flexible substrates and virtual labs for analog electronic circuits.
e-mail: kcnmurthy@gmail.com