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Design of Power Efficient Dynamic Latch Comparator for High Resolution SAR ADCs

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Abstract- In today's high performance low power era, there is an increasing demand for a power efficient comparators with high accuracy at moderate conversion speed for ADC, DAC and bio-potential acquisition system applications. This paper presents the design of power efficient dynamic latch comparator using inverter based preamplifier to overcome offset errors for enhancing the performance. The technique along with preamplifier using inverter topology limits the noise against inaccuracy issues like random offset errors and quantization error by reducing the common mode input voltage, V_{cm} and also, preserves the power efficiency when extending the effective number of bits (ENOB) bits for high resolution ADCs. The simulation is performed using 180nm CMOS process technology in Mentor Graphics. Proposed dynamic latch comparator outperforms the conventional dynamic comparators in terms of low power consumption with high resolution for ADCs.

Index Terms- Common Mode Input Voltage, Offset, Power Consumption, Preamplifier, Resolution.

1. INTRODUCTION

Nowadays, the bio-potential acquisition systems play a vital role in the improvement of health care scenarios. Wireless IoT wearable devices operate on biomedical voltages which are transformed to the digital form reliably using IC design. The successive approximation register (SAR) type analog to digital converters (ADC) are suitable to handle biomedical signals of low frequency bandwidth for such applications [1].

Comparator is a basic building block in overall performance of ADCs to keep a high resolution under adverse environments. The block diagram of the comparator in [2] is composed of the pre-amplifier and regenerative latch stage. This high resolution comparator reveals a multistage arrangement for high gain where each stage consists of a low gain amplifier but it consumes more power. Dynamic comparators are suitable to reduce the static power consumption in such applications. It operates on dynamic logic with respect to clock and it consumes less power compared to traditional comparator without clock. The offset voltage and positive feedback for latch are key design factors to enhance the performance of these comparators. Also, the disturbance from the positive feedback, known as Kickback noise should be reduced to improve the performance.

The preamplifier stages are involved for reducing the latch offset voltage to produce large output voltage from a small input voltage differences. Also, this reduces the kickback noise and other inaccuracy issues. The technique was proposed based on load latch approach in the preamplifier stage to reduce the power and offset and gives the improved result [3]. However, the multiple phases of clock circuit consume additional power. Another technique was proposed based on continuous scaling technology for same purpose [4]. Unfortunately, there exists large static power consumption and lower intrinsic gain in the preamplifier stage due to the decrease in source to drain resistance. The analysis depicted that conventional comparators are degraded with inaccuracy issues like mismatches of external load capacitances and internal parasitic and random offset errors [5]. In general, the systematic offset variations arise in the preamplifier and Latch stages due to the output currents mismatch in the output transistors. As consequences, the DC gain and number of preamplifiers must be increased as offset voltage increases [6]. The high sensitive preamplifiers are the solution to overcome such noise and other inaccuracy issues with low power consumption for high performance of dynamic latch based comparators.

The effects of common-mode input voltage V_{cm} of the comparator are discussed [7]. The choice of Vcm depends on a trade-off between the offset voltage, noise like random, leakage currents and kickback noise, power consumption, area and speed. Among the many characterizing parameters, the offset voltage of a comparator has a more impact on the monotonicity characteristics of the A/D conversion process and hence, auto-zeroed technique was proposed to realize offset cancellation [8]. However, it is designer choice to optimize the dynamic comparator based on the different specifications and applications of the design. For example, for high-resolution with moderate speed applications, it is good choice to reduce Vcm for cancelling the comparator noise. In the next design choice, it is difficult to preserve great power efficiency when increasing the range of effective number of bits (ENOB) beyond 10 bits for high resolution ADCs. The main reason is that resolution of ADCs is thermal noise limited. Also, it demands 4 times the analog power to reduce the thermal noise for every 1-bit. The SNR enhancement technique was proposed based on the estimation of conversion residue to reduce the noise and quantization error of the comparator for high

resolution ADCs [9]. However it requires high hardware complexity to estimate the conversion residue to compute the repeated LSB comparisons.

Thus, a novel power efficient dynamic latch comparators using inverter based preamplifier is proposed to overcome the inaccuracy issues and improve the performance for the applications that demand a low power and high resolution with moderate speed. The paper is structured as follows. The section 2 describes the existing and proposed dynamic latch comparators. The section 3 shows the simulation and performance comparison results. Finally, the conclusion is given in section 4.

2. SYSTEM DESCRIPTION

2.1. Conventional Dynamic Latch Comparators

The dynamic latch comparator as shown in Fig. 1 is attractive due to its many operational benefits such as zero static power dissipation, high speed, full voltage swing output and high input-impedance [10]. The main limitation is that current control enabled by only one tail current transistor M11 for the differential amplifier input pair, M5 and M10 and the latch using transistors M3, M4, M8 and M9. The tail size should be improved to drive a latch with high current but it disturbs input transistors during the transitions in the saturation region.

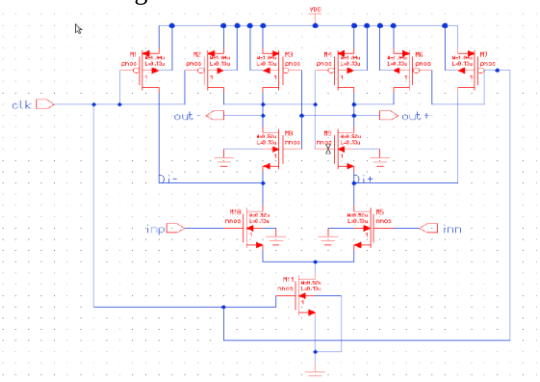

Fig. 1 conventional dynamic latch comparator

As an alternate, the comparator as shown in Fig. 2 uses two kind of differential stages for input amplification and output latch [11]. The comparator considers input offset voltage as design factor but the clock skew effects limits the performance. It needs an additional inverter block to produce the clock signals. This results in large delay and area and more power consumption. As a consequence, the demand on low offset needed a preamplifier circuit with large gain and transistor sizing. This requires huge amount of additional power and there is a tradeoff between area and power and latch offset voltage in this topology.

2.2. Proposed Dynamic Latch Comparators

Because the offset of the dynamic comparator has a great influence, inverter based preamplifier is proposed as shown in Fig. 3 for low offset and noise cancellation. It supports low power consumption and simplified circuit. The DC gain and bandwidth of the proposed inverter are exploited where it is maximized in the weak inversion region and it is saturated in the strong inversion region. Voltage regulator, not shown here, which control the Vdd of the inverter, provides the isolation for the inverter-based preamplifier against analog power line to achieve a high DC-gain and wider bandwidth. Thus, the design enhances capability to reduce the noise and circuit disturbances. This maintains the accuracy of the proposed comparator against offset variations.

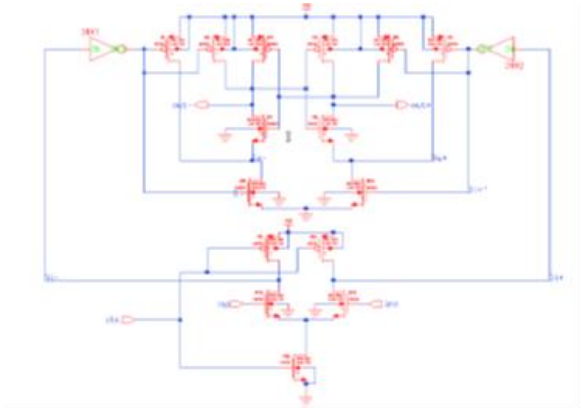

Fig. 2 comparator for low offset voltage

Because of the pull-push inverter arrangement of the MOSFETs (M11-M12 and M13-M14) and the complementary relation between the current and voltage Vdd of the comparator, it consumes the current only during the crossing region when switching and this ensures low power capability. Thus, the trade-off between power and offset is optimized. Nevertheless, it is difficult to maintain the power efficiency with respect to thermal noise when increasing the number of ENOB bits for high resolution because, the resolution of ADCs is thermal noise limited. In this regard, the effects of common-mode input voltage, Vcm are studied for the improving the performance of comparator. It is revealed that Vcm is reduced to minimize the noise effects for high-resolution with moderate speed applications. Thus, the rigid way of reducing the comparator thermal noise is relaxed and it leads to sustain the power reduction of the comparator.

3. SIMULATION RESULTS

The transient behavior of the proposed dynamic latch comparator is depicted in Fig. 4. The performance of proposed dynamic latch comparator is evaluated and compared with existing dynamic-comparators [10, 11]. The summary of performance comparison results is shown in Table 1. It explores the variation in parameters that are characterized with propagation delay, power consumption, number of transistors for implementation and ENOB for resolution of 12 bits for the supply voltage of 1.2 V. All the circuits are simulated using Pyxis tool (Mentor Graphics) at 180nm CMOS process technology. The proposed

design brings low power consumption due to DC gain of the inverter based preamplifier topology as it consumes the current only during the crossing region. This achieves low power consumption when compared to the conventional comparators. The improved quality of proposed technique is depicted in terms of lower power consumption and optimized delay value.

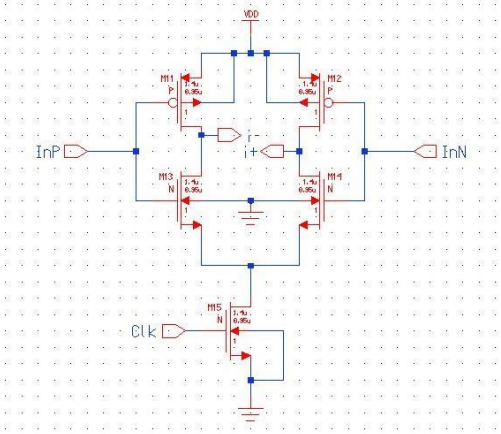

Fig. 3 schematic of inverter based preamplifier for proposed comparator.

The design of the comparator is developed to consider resolution of 12 bits for SAR ADCs. The input stated noise of comparator is around 500μV. The design should reduce noise to .13 LSB and quantization error to .24 LSB for the target of maintaining the total noise below .37 LSB. For every operating regions of the proposed preamplifier, the latch intrinsic offset is below 1 mV due to open loop DC-gain and higher bandwidth against offset and noise variations. Thus, the trade-off between power and offset is optimized and it indicates good reliability of the proposed comparator with high power efficiency. The loss of 0.5 bits is reported when extending the ENOB of more than 12 bits due to robust design of the proposed comparator which maintains high power efficiency and low Vcm under offset and noise variations.

The same orientation of transistors and symmetry of circuit are developed to optimize for the compact area. It needs only two additional transistors for inverter based preamplifier of the proposed comparator and so, implementation complexity is simplified. Thus, it is concluded that proposed comparator provides high performance as compared to traditional dynamic comparators.

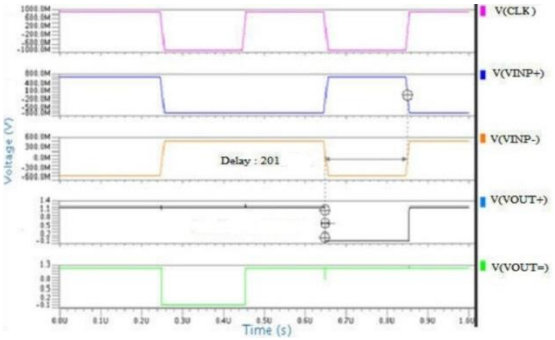

Fig. 4 signal behaviour of proposed comparator

Table 1: Performance comparison of different comparators

Specification	Conventional Multistage Comparator	Conventional Dynamic Latch Comparator	Comparator for Low Offset Voltage (1)	Proposed Comparator
Process Technology	CMOS, 180nm	CMOS, 180nm	CMOS, 180nm	CMOS, 180nm
Supply Voltage	1.2 V	1.2 V	1.2 V	1.2 V
No. of Transistors	23	11	19	21
Power Consumption	3.78 μW	0.7 μW	1.2 μW	0.9 μW
Delay	150ns	260 ns	201 ns	201 ns
ENOB for Resolution of 12bits	9.05	10.5	10	11

4. CONCLUSION

The dynamic latch comparator using inverter based pre-amplifier has been introduced for the power efficiency and performance improvement against inaccuracy issues. The proposed design is powered by 1.2V supply and the output signal exhibits 201ns delay and utilizes optimum number of 21 transistors which is optimized related to the other works. The proposed comparator consumes optimum power of 0.9 μW to achieve 11 bits of ENOB and thus, fit for low power high resolution applications. The results show that the proposed comparator outperforms existing dynamic comparators in terms of low power consumption with high resolution at moderate speed for ADCs.

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