International Journal of Research in Advent Technology, Vol.7, No.4S, April 2019
E-ISSN: 2321-9637
Available online at www.ijrat.org

OPTIMIZED AREA EFFICIENT DIGITAL MATCHED FILTER

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ABSTRACT: Digital Matched Filter (DMF) is the key component of fast Pseudo Noise (PN) Code synchronization in Direct Spread- Spectrum Systems (DSSS), and its realization is a crucial technology of digital DSSP receiver. For long PN code DMF needs a mass of hardware resource, recursive delay chain, folded DMF and Time-Division Multiplexing are used to optimize FPGA realization of DMF to reduce the consumption of FPGA resource, which would reduce the cubage and cost of the receivers'.
Index Terms: digital matched filter, recursive delay line, folded DMF, time-division multiplexing..

1. INTRODUCTION

With development of DSSS communication technology[1] and software radio technology, all digital spread-spectrum receivers have become focus of research.. Receiving of direct sequence spread spectrum system usually adopts relevant receiving means, which mainly completes two courses as despreading and demodulating. Usually, first is to despread then to demodulate, first de-spreading can acquire spread-spectrum gain via de-spreadingcourse,thus, S/N (signal-to-noise) and C/I (carry-to interference) of demodulator[2] can be increased, and anti-jamming capability of the system can also be strengthened. When direct sequence spread spectrum system is de-
spreading, first completing spreadspectrum code in-phase, then conducting relevant despreading upon spread-spectrum signal by using the same code sequence. Velocity and phase of receiver local spread-spectrum code must be in consistent with received spread-spectrum sequence. When physic difference between transmitting end and receiving end
is more than 1 CHIP code, their relevance will no longer exists. The first step of de-spreading is to capture a phase status which complies with local spread-spectrum code in received signals. Phase capture in spread-spectrum sequence can usually be reached by using matching filter or phase search circuit, and capturing speed of matching filter is the highest. DMF is the core element of all digital spread-spectrum receiver, and mainly used in PN rapid capture and de-spreading. Traditional DMF design efficiency is quite low, when PN code length L is quite big, it needs to occupy much FPGA source, and the cost is substantial. The author puts forward DMF recursive folded structure by improving delay line structure and combining TDM (time division multiplexing) technology. And this structure extremely reduces resource consumption of DMF.

2. CONVENTIONAL SYSTEM

2.1 Dmf Basis Structure And Parameters

DMF is a special FIR filter of which tap spacing is chip sequence and tap coefficient is spread spectrum. And its direct form[3] is composed of delay line and relevant calculation units (CCU). see fig.1.

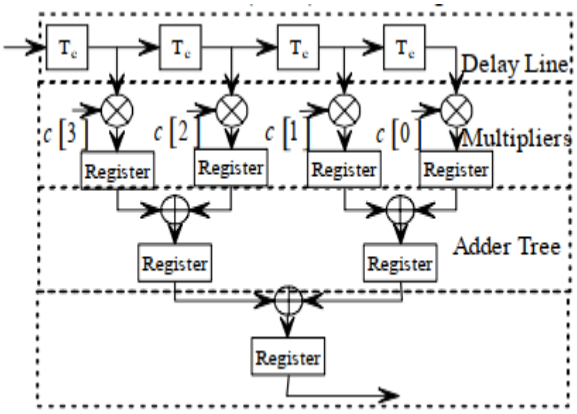


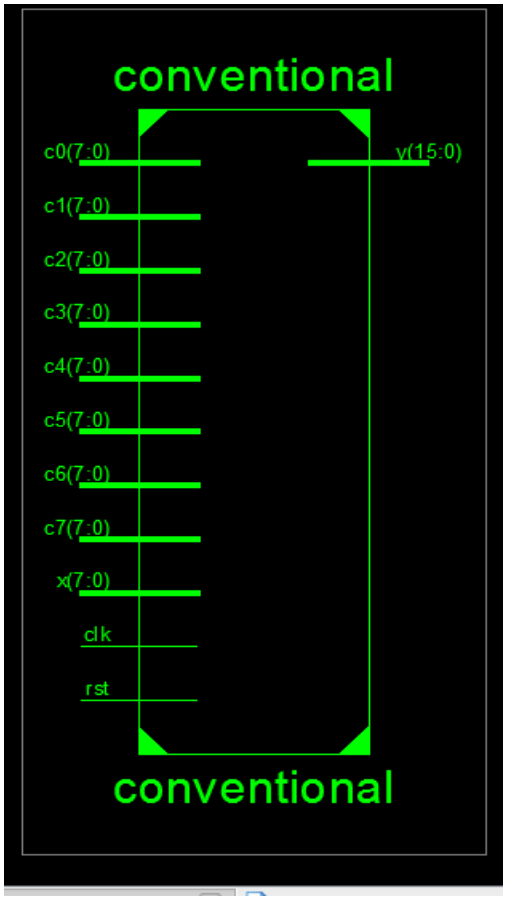
Fig 1.Direct form structure of DMF

Delay line is used to save all input samples within relevant time scope (LTC), and composed of number of L delayed units. Level connection of multi D trigger is the simplest method of realizing delay unit, but it will use numerous D triggers, therefore, it is not applicable for constituting DMF delay line of which digit is big and step is high. FPGA possesses rich LUT resources. It can realize 1-16 times signal delays by using 16bit recycling shift register[4] (SRL16E). As for DMF of which M bit quantification and over sample times, constituting a delay unit needs SRL16E.

As fig. 1, relevant calculating unit is composed of L multipliers and one inversed pyramid additive tree. And the first grade of additive tree has L 2 ( ) M+1 bit two input in-phase adder (what participates calculation is delay tap sample, word

length is M bit, in order to prevent computing overflow, it needs to extend 1 bit symbol position before adding), the second grade has L 4 (M+2) bit two input inphase adder……, and the entire additive tree has L-1 two input in-phase adder.

Recursive folded DMF put by the author fully utilizes storage potentiality of SRL16E, using recursive structure to reduce delay line resource consumption, then using such features of recursive delay line as tap de-multiplies while tap sampling velocity multiplies to time division multiplex relevant computing units, so as to reduce quantity of adder and multiplier. Above stated measure can reduce hardware resources consumed by DMF in multiplying way.



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	87	4656	1%
Number of Slice Flip Flops	168	9312	1%
Number of 4 input LUTs	112	9312	1%
Number of bonded IOBs	90	232	38%
Number of MULT 18X 18SIOs	8	20	40%
Number of GCLKs	1	24	4%

3. PROPOSED SYSTEM

3.1 Structures And Features Of Recursive Delay Line

Traditional delay unit uses SRL16E to realize R (R 16 ≤) shift registration. In every sampling period (TS), all R sampling in the delay unit shift one digit rightward, thus, input sample is shifted to tap place through R T × S , so that TC time delay has been realized. R Shift place processing fails to extensively utilize storage potentiality of SRL16E, therefore, the author puts forward recursive delay line structure. In such structure, whatever value R is defined, SRL16E will conduct 16bit shift processing. Therefore, storing L R × input sample needs Mx L xR/ 16 × × SRL16E, which is only R 16 of traditional structure. Now, let's conduct timing analysis by combining in below fig.2

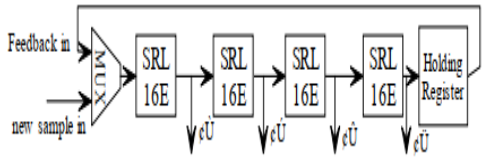


Fig 2.Structure of recursive delay line

Because SRL16E conducts 16bit shift processing, in order to secure its timing delay to equal TC , shift period must be T 16 C .Defining R T 16 × S as work clock period of delay line, then work clock frequency *fCLK*is 16 times of chip velocity, namely C times of sampling rate, among which C= R 16 , therefore, a new sample shall be input every C work
clock period. Here we assume that new sample comes in *n*C work clock period (moment for short hereinafter), among which *n* is integral. If moment *m* is integral times of C , MUX drives new sample into delay line, otherwise MUX feedback old sample in the holding register to the input end of delay line.Recursive delay line only needs L C delay units to realize L T × C delay, at the cost of increase C times of work clock frequency, and resource consumption is thus compressed to 1 C of that before optimization. For example, when R=4 , C=16 R 4 = , namely resource consumption is only 25% of former value.

3.1.1 Recursive Folded Dmf (1/2)

Recursive delay line not only reduces tap number to 1 C of that before optimization, but also output velocity of tap sample increases by C times. Corresponding with it, number of multiplier and adder in relevant computing units respectively reduce L and L-1 to L C and L C-1 , in the meantime, work frequency increases by C times. Within C work clock period, relevant computing units compute some relevant values of receiving signal and PN sequences at C phases by turns according to signal phases decomposed by recursive delay line,andcompleting combination of

some relevant values by using accumulator, so as to acquire complete relevantvalue. According to this way of thinking, the authorputs forward recursive folded structure which is as following fig. This structure folds and uses relevantcomputing units on the basis of recursive delay line, sothat using one L C tap DMF to complete steps matching filter calculation.

Fig.3 is a 1/2 recursive folded filter, it uses 1 4-tap DMF timing division to realize 8 steps matching filter, its parameters are L=8 , R=8 and C=2 .Timing analysis is similar to previous section. Consistent as usual situation, assuming to drive new sample to delay line at even moment MUX, and MUX feeds back sample which is held in register to entrance of delay line at odd moment. After a short period, output sample of a certain tap at odd moment will lag behind half code phase period with that of next moment, therefore, in neighbouring clock period, multiply coefficients which have been loaded to each taps will also lag half code phase period. Accumulator merges some odd and even moment's relevant values, so as to get entire relevant values.

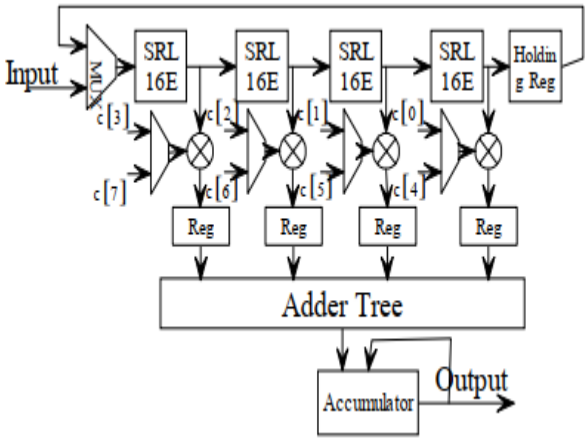
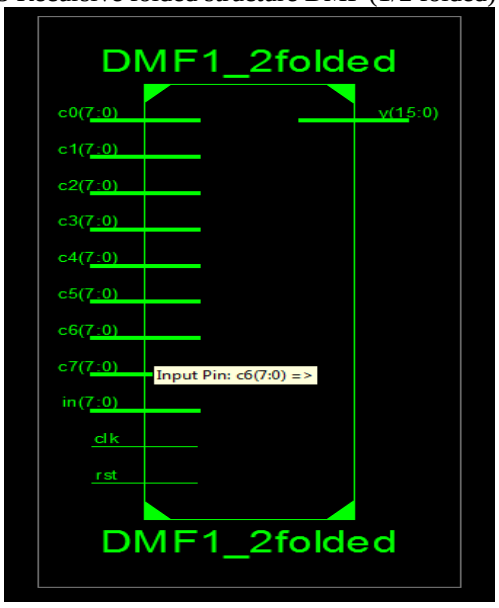


Fig.3 Recursive folded structure DMF (1/2 folded)



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	25	4656	0%
Number of Slice Flip Flops	16	9312	0%
Number of 4 input LUTs	16	9312	0%
Number of bonded IOBs	18	232	7%
Number of GCLKs	1	24	4%

3.1.2 Recursive Folded Dmf(1/4)

Fig.4 is structure framework of 1/4 recursive folded filter （L=8 , R=4 and C=4 ）.Timing is getting more complicated, in neighbouring clock period; phase difference between tap samples is 1 4 code period.

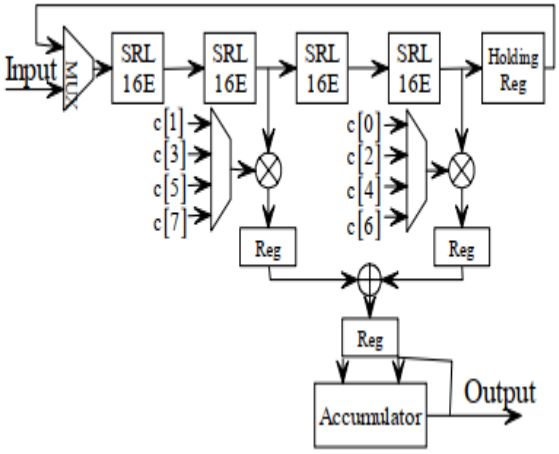
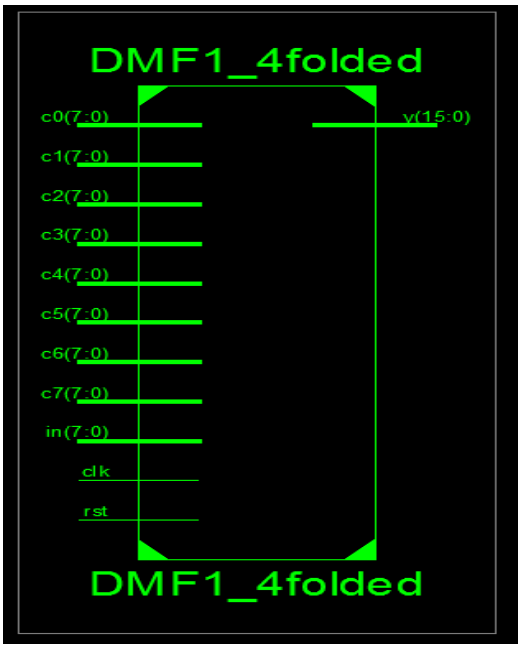


Fig.4 Recursive folded structure DMF (1/4 folded)



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	8	4656	0%
Number of Slice Flip Flops	16	9312	0%
Number of 4 input LUTs	16	9312	0%
Number of bonded IOBs	18	232	7%
Number of GCLKs	1	24	4%

4. RESULTS:

COMPARISON TABLE FOR THE RESOURCE CONSUMPTIONS OF DMF

DESIGN	SLICES	LUTS	FFs
CONVENTIONAL	**87**	**168**	**112**
½ FOLDED	**25**	**16**	**16**
¼ FOLDED	**8**	**16**	**16**

The above table tells us, conventional method consumes more resources compared to other DMF systems which is undesirable. For example, for Xilinx Spartan3E series FPGA, when chip velocity is less than 10 MHz,you can choose 1/ 4 or 1 /2 recursive folded structure, at this moment, work frequency is also less , timing should be moderate.

5. CONCLUSION

Using the theory of mutual exchange between clock frequency and design size, via recursive delay line, folded relevant computing unit and timing division multiplexing technology, recursive folded structure remarkably reduces DMF resource consumption. Using the theory of mutual exchange between clock frequency and design size, via recursive delay line, folded relevant computing unit and timing division multiplexing technology, recursive folded structure remarkably reduces DMF resource consumption. Nd this structure has been applied in a certain type intermediate frequency digitalized direct-sequence spread-spectrum receiver, and achieved good result, the optimizing effect is very remarkable. Under the condition that sampling rate is 40.96MHz, work clock frequency is 163.84MHz, through 4 times timing division multiplexing and its resource consumption is about 1/3 of that before optimization.

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