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Optimization of MAC unit using full pipelined accumulator

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Abstract-This paper emphasizes on the contextual details of the optimization of the combination of two basic units used for computation i.e. multiplier and accumulator unit. In the past few years, real-time signal processing and digital signal processing has emerged with an unstoppable pace which in turn developed the need for low power and high throughput circuitry. In digital processing systems, the MAC unit plays a vital role as it decides the speed of the system thereby determining its actual throughput. The proposed model comprises a multiplication unit which ultimately briefs the variable performance parameters of the system. Foremost we did a comprehensive study about the various multipliers that could be used to enhance the speed and provide high throughput for a digital system. The MAC unit is a combination of three basic units viz. multiplier, accumulator and an adder. In the present MAC units, there is a high delay problem which has limited its efficiency to some extent. In this research work, we made the utilization of carry save adder to control the various parametric constraints to improve its efficiency, feasibility and computational effectiveness as compared to the existing methods. We used the array multiplier to reduce the propagation delay as it has various inputs in parallel which proved the best for pipelining. The VHDL code used in this research work in synthesized on Xilinx and simulated on Modelsim.

Index Terms-Multiply-accumulate (MAC) unit, array multiplier, carry save adder, optimization, delay, power.

1. INTRODUCTION

Every digital signal processor contains the MAC unit. The MAC unit does the multiplication and accumulation processes continuously in order to perform repeated complex operations in digital signal processing. Multiplication-and-accumulate operations are the basics for digital filters. Therefore, the functionality of the MAC unit ensures high-speed filtering and other processing necessary for DSP applications. Since the MAC unit operates fully independent of the CPU, it can execute data separately and thereby reduce CPU load. A major application like optical communication systems which is based on DSP, require extremely fast processing of a large amount of digital data. A MAC unit comprises a multiplier and an accumulator containing the sum of the previous successive products. The MAC inputs are achieved from the memory location and given to the multiplier block. The existing MAC unit models reviewed are designed using Verilog HDL, simulated and synthesized using Xilinx. Several methods for optimization of multiplier-accumulator (MAC) unit have been proposed in the recent literature. This paper mainly focuses on array multiplication process to reduce the power consumption, increasing speed, reducing CPU load and implementing a fast multiplication network. However, there is a huge variety of techniques to implement the MAC unit for overcoming the limitations of earlier methods implemented. This paper provides a comprehensive analysis of the major techniques and an intense classification based on speed, power requirements and efficiency.

2. LITERATURE REVIEW

In this section we concisely discuss various previously done research work related to MAC unit:

M.Nasiruddin, Dr. Prashant Sharma, Dr. Vijay Chaurasia, "Implementation of optimized multiplier-accumulator (MAC) unit with Vedic multiplier and full pipelined accumulator: a review" presented a deep analysis on the concept of Vedic multiplier with reviewing the various existing methods to implement Vedic multiplier for accumulator design.

P. SivaNagendra Reddy, M. Saraswathi, "Design and Implementation of FPGA based 64-bit MAC unit using vedic multiplier and reversible logic gates" describes Multiply and Accumulate Unit using Vedic Multiplier and DKG reversible logic gates.

G. Priyanka, D. Poornachandra Reddy, "Implementation of MAC Unit by using Modified Wallace Multiplier For DSP Applications" presented in International Journal of Scientific Engineering and Technology Research, describes an efficient

implementation of a high speed parallel multiplier using both these approaches.

Prof.Tariquzzaman, Prof. M. Nasiruddin, "Design of High Speed and Low Power MAC Unit with Vedic Multiplier and Full Pipelined Accumulator" proposes the technique of low power MAC unit with Vedic Multiplier and full pipelined accumulator to boost the speed and reduce power dissipation.

Different researchers proposed different methods to optimize various characteristics such as power, delay, throughput and processing area requirements. Among all these methods multiply-accumulate (MAC) unit using full pipelined accumulator proved itself as the most efficient technique to reduce the power consumption. This proposed method represents the 32-bit MAC design using full pipelined accumulator by making use of array multiplier.

3. PROPOSED METHODOLOGY

MAC unit plays the most important role when it comes to digital signal processing (DSP) applications. The MAC unit comprises a multiplier, an adder, and an accumulator. These three blocks when working together, they are considered as a multiply-accumulate unit. In this paper, we made use of 32-bit array multiplier. The inputs to the array multiplier are obtained from the memory locations and given to the array multiplier which has 32-bit inputs. The concept of array multipliers is based on the shifting and add procedure. This will be useful in 32-bit digital signal processing units. The two inputs of 16 bits each are applied at the input of multiplier.
When the input is fed to the multiplier it starts the multiplication process and the output comes out to be 32 bits. The output of the multiplier is given to the adder circuitry which is basically a carry save adder. The function of the carry save adder is to store the carry for the processing of the next stages. The output of the MAC unit is obtained by the aforementioned equation:
$Y=\sum AiBi$
Where, Ai & Bi are the two 16 bit inputs.
Y gives the output.
In this case, the output of the carry save adder comes out to be 33 bit i.e. 32 bits from the multiplier output along with one carry bit (32 bit+1 bit).The accumulator which is also a storage register/buffer is implemented using parallel in parallel out (PIPO) approach due to the fact that carry save adder produces all the output bits in parallel. The parallel in and parallel out approach helps in the designing by considering all the inputs as parallel bits and generates the output bits in parallel. Finally the output from the PIPO accumulator is again fed back as one of the inputs to the carry save adder.
The architectural view of the designed MAC unit is shown below:

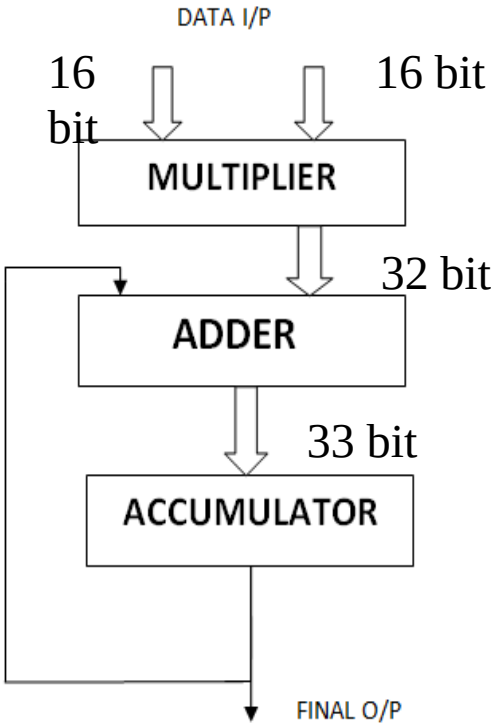

Fig 1: Architectural view of MAC unit

3.1. *ARRAY MULTIPLIER*

The combinational generation of all bits products and their summation with an array of full adders is a very good alternative to simple multiplication. The partial products are obtained and stored by an array of adders just after the multiplier. An n x n array multiplier has the requirement of n(n-1) adders and the number of AND gates equals to n^2.

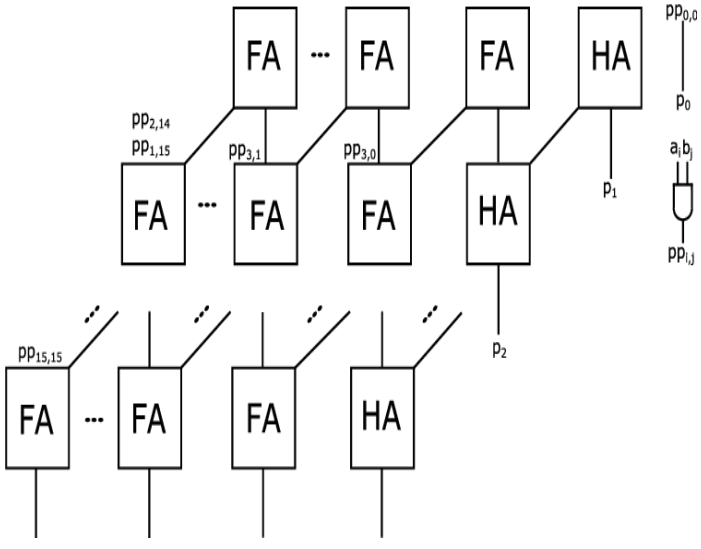

Fig 2: Block Diagram of 32 bit array multiplier

4. RESULT

The proposed MAC unit model is designed using Verilog HDL and synthesized using Xilinx ISE 13.2 for Virtex-6 family device. The simulation result of proposed multiplier-accumulator (MAC) with improved speed and less delay for real time digital signal processing (DSP) applications.

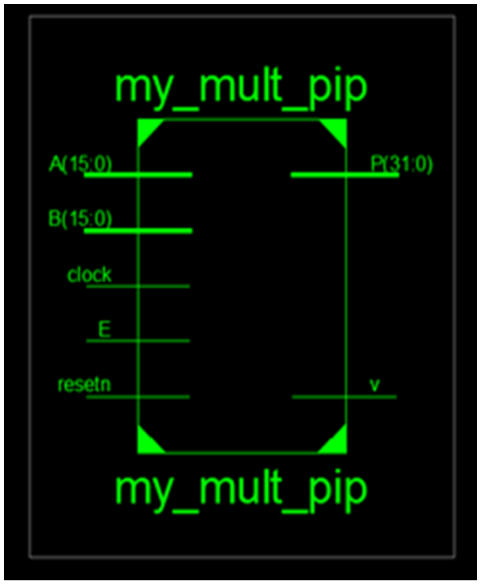

Fig 3: RTL schematic of proposed MAC unit

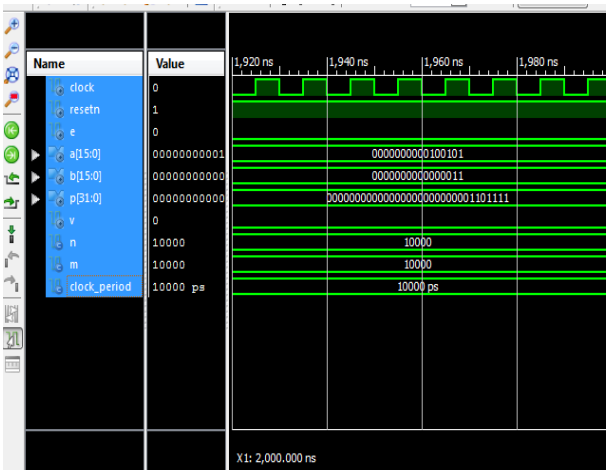

Fig 4: Simulation results of MAC unit

5. CONCLUSION

In this paper we proposed a MAC architecture based on array multiplier with special focus on the reduction of power which in this case has reduced to 0.14 W for 32-bit MAC.We have gone through numerous techniques to implement the MAC architecture with the least delay and power requirement capabilities.The concept of array multiplier with carry save adder for the development of this proposed MAC unit have given good results in terms of its power efficiency.

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