

An Asymmetrical Multilevel Inverter Model with minimum power electronic components

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Abstract- In this paper, a novel cascaded multilevel inverter is being proposed without using a full bridge inverter module. By arranging the input dc sources in a proper sequence, this proposed system eliminates the role of the full bridge inverter module. This paper is mainly focusing on the number of power switches used in order for the particular level output. The main advantage of this proposed model is its simplified structure which leads the proposed structure to be more compact. Two different input voltage patterns have been described here for the proposed scheme. For each voltage pattern, different voltage output levels are obtained. The output voltage level can be increased effectively by choosing the proper input voltage magnitude. It uses only the asymmetrical mode of configuration. Its simulation and experimental results verify the operation and performance of the proposed system. Finally, the comparative analysis has been made with some recently developed topologies to ensure the effectiveness of the proposed system.

Index Terms- *Asymmetrical configuration, Cascaded multilevel inverter, Full bridge inverter, Full stepped converter*

1. INTRODUCTION

The Multilevel inverter plays a significant role in DC-AC power conversion. It is getting more attention because of its modular structure. The renewable energy sources like Fuel Cells, PV Cells and Supercapacitors are producing DC supply. Hence it needs an interfacing module to connect to the AC loads. The connected module should possess the property of high-quality energy conversion. In such cases, Multilevel Inverter is one of the best choices for such interfacing applications. The applications of the Multilevel Inverters are not limited to the interfacing module. It is also used in various high voltage applications such as hybrid electric drives, Voltage restorer, FACTS and Compensating devices, etc. [1]-[3].

The Multilevel Inverter is one of the Static Power Conversion devices, and it produces the stepped output voltage waveform from the arrangement of different dc input sources. The input dc voltages may be obtained from various sources. Due to its application areas, these inverters are getting more attention, and more researches are carried out in this field. Different new topologies and a wide range of control strategies have been introduced in the last few years. The multilevel inverter is capable of producing

the output voltage with smaller steps and low harmonic content which are the significant advantages of these inverters. These inverters are classified into three different categories. They are (i) Flying Capacitor Multilevel Inverter [4] (ii) Diode Clamped Multilevel Inverter [5] and (iii) Cascaded H Bridge Multilevel Inverter. The types mentioned above have its advantages as well as disadvantages too.

The flying capacitor multilevel inverter requires several storage capacitors if it is designed for high-level outputs. These high power capacitors are more expensive, and the entire circuit is considerable. The control of such inverter becomes highly complicated and more losses are raised during the real power transmission. The control scheme for the Diode Clamped multilevel inverter is simple. But these types of inverter requires more clamping diodes during high output levels. The control of real power flow is often difficult in this case. These two types of inverters have some restrictions to use it for high voltage applications [6].

The cascaded H Bridge multilevel inverter produces the stepped voltage waveform by connecting the number of Full bridge inverter in series. Each inverter is supplied through the separate DC sources. This type of inverter does not require any additional Diodes and

Capacitors. By the modular structure and ease of control, the cascaded multilevel inverter can be used for the high voltage applications while comparing with the other two types; this cascaded inverter requires the minimum number of switching components. The number of Full bridge inverter requirement will be more when the output level is high.

The switching losses and harmonics are increased if a number of switching devices used in the inverter. The various symmetrical and asymmetrical inverters introduced in [7]-[9] uses a minimum number of dc input sources, but require more power switches. Hence the circuit becomes more complex, and it effectively increases the cost of the inverter. The topology introduced in [10] uses sub-multilevel converter concept to generate the stepped output waveform. Three different methods of input voltage magnitude calculation also been presented. The significant advantage of this asymmetrical configuration uses an only minimum number of dc sources. But the major drawback is the cascade connection of the basic unit, which increases the number of switches utilized.

The multilevel inverter introduced in [11]-[12] uses a series/parallel voltage concept by the switched capacitor to produce the stepped output. The significant disadvantages in this concept are a number of switches and capacitor used. The idea introduced in [13]-[14] uses sub-multilevel inverter module for generating actual stepped output. The full bridge inverter is used for creating a positive and negative peak. The advantage of this concept is it requires one full bridge inverter module; thereby it avoids the cascade connection. But the number of switches used will be high is its major drawback. The topologies introduced in [15]-[17] are also using switch reduction concept. But the number of power switches used remains high in all those modules.

This paper introduces a new asymmetrical inverter which avoids the usage of full bridge inverter in the cascaded multilevel inverter. By making necessary changes in the voltage inputs and switch arrangements on the existing systems the required stepped output voltage can be generated easily without using a full bridge inverter module. The elimination of the entire bridge inverter module in the proposed scheme leads to the utilization of a minimum number of power switches. The proposed module is described with two different input voltage patterns. For simplicity, among

the two different designs, the results of the two schemes are discussed. Finally, the comparative chart for the number of switches utilized in the proposed plan with some existing systems is also included.

2. PROPOSED TOPOLOGY

This chapter describes the proposed cascaded multilevel inverter. It consists of series-connected individual cells together form a full stepped converter. This total stepped converter directly connected to the load. Each cell comprises an input voltage source and a pair of switches. The switches are used to connect or disconnect the corresponding input voltage to the charge. The general topology of the proposed multilevel inverter is shown in Fig. 1. The switching devices connected to the input source should be in the proper way, otherwise chances of distorted output. This is because each semiconductor switch has its freewheeling diode, during the off state of the particular switch the corresponding input source may be connected to the load through the freewheeling diode. Hence the switches are arranged in a correct sequence to avoid the conduction of the freewheeling diode.

The input voltages are arranged in both forward and reverse direction as per the requirement. The reverse input voltage is to ensure the output voltage in the negative half cycle. The full bridge inverter module is not used in the proposed scheme. Hence some of the voltages are connected in the reverse direction. The input sources are connected to the load through a pair of switches. These are grouped into two categories namely odd and even set of switches. Both switches are operated in a complementary mode. Whenever the odd set switch comes to the ON state, the input voltage will be connected to load. Otherwise, the load is disconnected from the source.

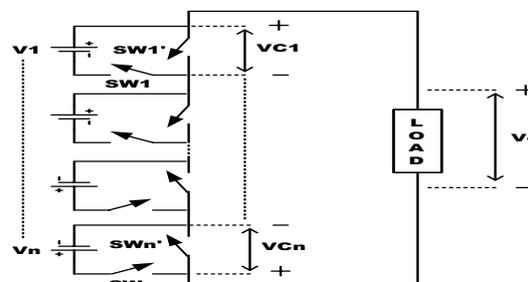


Figure 1. General Structure of the proposed multilevel inverter

In this state even set switch comes to ON state. The generalized output voltage of the multilevel

inverter is given in Fig. 2. Hence both switches will not come to ON state at a particular time in an individual cell. V_{c1} , V_{c2} denote the voltage outputs of the individual cells... V_{c_n} the input voltages connected in the opposite direction deliver the negative output. Since these voltages are connected in reverse direction to the load. Similarly, the net output voltage of the proposed multilevel inverter is the sum of individual cell voltage, and it is described as follows.

$$V_o = V_{c1} + V_{c2} + \dots + V_{c_n} \quad (1)$$

Depending upon the input voltage arrangement, the corresponding voltage inputs are taken as either a positive or negative magnitude. For simplicity, in this paper, the number of an input voltage is limited to four. For the proposed multilevel inverter two different voltage patterns are discussed here.

2.1 Voltage pattern 1

For the proposed multilevel inverter this voltage pattern is used to generate the 11 level output. Four input voltage is applied in this scheme. Among them, two voltages are connected in the reverse direction. The structure of the proposed 11 level inverter is shown in Fig. 3. The voltage magnitudes of these four voltages are taken as follows, $V_1=20V$, $V_2=30V$, $V_3=10V$, $V_4=40V$. The voltage inputs V_3 and V_4 are connected in the reverse direction, hence both they should be taken as a negative voltage. The individual cell voltages are taken as V_{c1} , V_{c2} , V_{c3} , and V_{c4} .

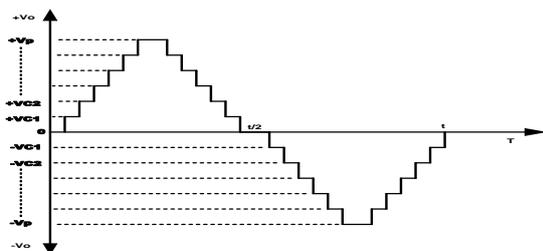


Figure 2.A generalized output voltage of the multilevel inverter

For the 11 level inverter with the step value of 10V, the peak to peak value should be of 50V. Hence to produce the peak to peak voltage of 50V in positive steps, the voltage inputs are taken as 30V and 20V. Similarly, for the negative actions, the voltage inputs are taken as 40V and 10V. For the output step of positive 10V, the sources V_1 and V_3 has to be connected in series by turn ON the switches Sw_1 , Sw_4 , Sw_5 , and Sw_8 .

On the other hand, the switches Sw_2 , Sw_4 , Sw_5 , and Sw_8 are in working state to produce the negative step of 10V. The switching state for the proposed 11 levels

multilevel inverter is given in Table 1. This switching table provides the switching states of the power switches during each step of the output voltage.

2.2 Voltage pattern 2

The input voltage arrangement of the proposed multilevel inverter for the second voltage pattern is shown in Fig. 4. In this pattern, voltage (V_4) is alone connected in the reverse direction. Hence it should be considered as a negative voltage. For the 15 level output, with 10v step the peak to peak voltage is varied from +70V to -70V. So the voltage magnitudes are taken as $V_1=10V$, $V_2=20V$, $V_3=40V$, $V_4=80V$. To generate the output voltage of +50v the switches Sw_1 , Sw_4 , Sw_5 , and Sw_8 should be in ON state. Similarly, the switches Sw_1 , Sw_3 , Sw_6 , and Sw_7 are in working condition to generate the output voltage of -50V. The switching state of the proposed 15 level inverter is given in Table 2. It provides the working states for each step. In this way, if the individual cells are increased the voltage output levels can be increased as 31 level, 62 level, and 124 level, etc.

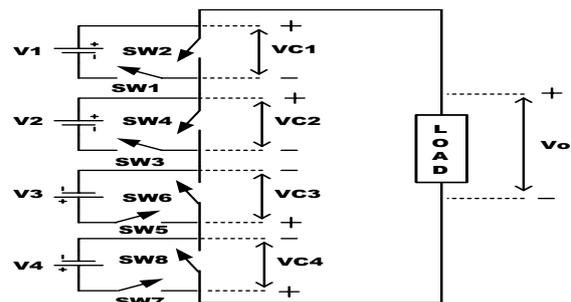


Figure 3. Structure of the proposed 11 level inverter

Table I Switching States of the Proposed 11 Level Inverter

V_o	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7	SW_8
10	1	0	0	1	1	0	0	1
20	1	0	0	1	0	1	0	1
30	0	1	1	0	0	1	0	1
40	1	0	1	0	1	0	0	1
50	1	0	1	0	0	1	0	1
-10	0	1	0	1	1	0	1	0
-20	0	1	0	1	0	1	1	0
-30	1	0	1	0	1	0	1	0
-40	0	1	0	1	1	0	0	1
-50	0	1	0	1	1	0	0	1

3. SIMULATION MODELLING AND RESULTS

This chapter describes the Simulink model of the proposed multilevel inverter described in chapter II. The MATLAB Simulink environment is used here to validate the performance of the proposed multilevel inverter. The most important part of the simulation is the switching pulse generation. The power switches in the circuit operating according to the pulse given to it. If there is any mismatch in the switching pulse, then the distorted voltage will be obtained across the output. Efficiency and harmonic distortion can be controlled effectively by choosing appropriate pulse generation methods.

The Pulse Width Modulation schemes are the most widely used gate pulse generation technique. Various new schemes have been introduced in recent years [16]. The pulses are generated according to the switching states of the switches at each step. These values are of described in the corresponding switching tables in chapter II. The switching pulses are switched to the fundamental frequency. The sinusoidal pulse width modulation technique is used here to generate the switching pulses.

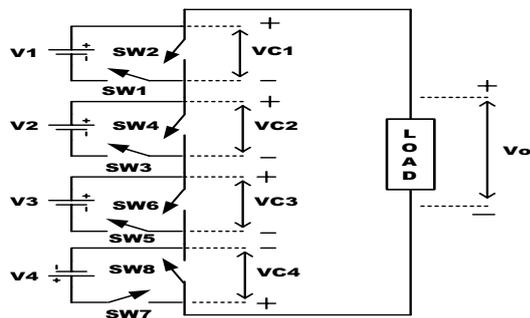


Figure 4. Structure of the proposed 15 level inverter

TABLE II SWITCHING STATES OF THE PROPOSED 15 LEVEL INVERTER

V_o	SW ₁	SW ₂	SW ₃	SW ₄	SW ₅	SW ₆	SW ₇	SW ₈
10	1	0	0	1	0	1	0	1
20	0	1	1	0	0	1	0	1
30	1	0	1	0	0	1	0	1
40	0	1	0	1	1	0	0	1
50	1	0	0	1	1	0	0	1
60	0	1	1	0	1	0	0	1
70	1	0	1	0	1	0	0	1
- 70	1	0	0	1	0	1	1	0
- 60	0	1	1	0	0	1	1	0
- 50	1	0	1	0	0	1	1	0
- 40	0	1	0	1	1	0	1	0

- 30	1	0	0	1	1	0	1	0
- 20	0	1	1	0	1	0	1	0
- 10	1	0	1	0	1	0	1	0

The gate pulses are generated by comparing the reference signal and the carrier signal. Among the two different signals, the carrier signals only adjustable. Its values are adjusted according to the switching sequences provided in the two tables. The switches in each cell are operated in a complementary mode, so it is enough to generate the gate pulse for any one of the switch. By including the inversion block, another switch will be operated. Here the pulses are generated only for the odd set of switches. By inserting NOT, gate block pulses are generated for the even set of switches.

3.1 Fifteen level inverter

The simulation diagram of the proposed 15 level inverter is shown in Fig. 5. The switches are arranged as per the structure is given in Fig. 2. The gate pulses have been generated according to the switching pattern provided in the respective table of the proposed scheme. For the circuit simplicity, the pulse generated circuits are masked in the subsystem. The generated pulses are connected to the gate terminal of the corresponding switches as shown in the simulation diagram.

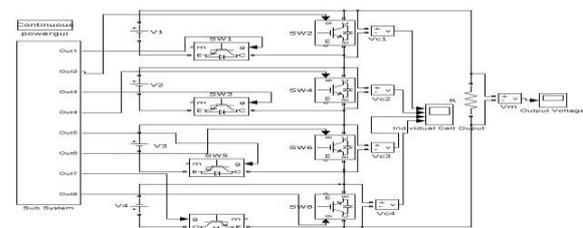


Figure 5. Simulation diagram of proposed 15 level inverter

The proposed system is simulated for the purely resistive load. In this scheme, only voltage input (V4) is connected in the opposite direction. Hence the voltage output of the fourth cell (Vc4) is obtained in the negative direction. The remaining voltages are obtained in a positive direction

The individual cells are combined together to form a full stepped converter. These cell voltages are connected to the load as per the switching signals applied to the corresponding switches. The net output voltage of the proposed multilevel inverter is obtained by the combination of these individual cell voltages. The 15 level output of the proposed system for R Load

is shown in Fig. 6. For the simulation system, the input voltage magnitudes are considered as 4V, 8V, 16V, 32V respectively. The individual cell voltage output is shown in Fig. 7. The output voltage shown in Fig. 8 shows the peak to peak voltage of 28V with a step value of 4V is obtained clearly as that of explained in its operation in chapter II.

Similarly, for the RL load, whose values are considered as 10 ohms and 10mH. The input voltages are taken here as 11.25V, 22.5V, 45V and 90V. The voltage and current output of this proposed scheme are shown in Fig. 8. The peak to peak voltage 78.75V with the step value of 11.25V gives the 15 level output as described.

4. EXPERIMENTAL RESULTS

This section describes the experimental results of the proposed system. The hardware setup of the proposed multilevel inverter is developed and verified practically. The experimental verification of 15 level inverter is carried for both R and RL loads. For the prototype, the power switching devices used here IRF640 type MOSFET with voltage and current ratings are 200V and 18A.

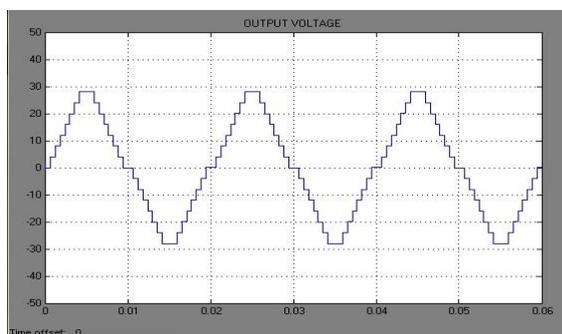


Figure 6. A simulated output voltage of the proposed 15 level inverter

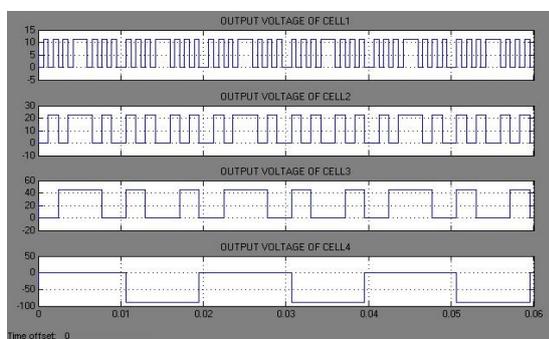


Figure 7. The individual cell voltage of the proposed 15 level inverter

The switching pulses have been generated by using the Atmega16 processor. The load current is of measured with the help of Hall Effect based linear current sensor (WCS1600). For the experimental model, the magnitudes of the voltages are considered as 11.25V, 22.5V, 45V and 90V. It can able to generate the peak voltage of 78.5V in both positive and negative magnitude with the step voltage of 11.25V. The sinusoidal modulation is used for the switching pulse generation since it leads to low switching losses. Fig. 9 shows the experimental results of the proposed inverter for the R load which is taken as 10 ohms. The simulated and experimental results have been a close agreement to each other.

5. COMPARATIVE ANALYSIS

This chapter describes the comparative analysis of the proposed scheme, and it is shown in Fig. 12. The proposed cascaded multilevel inverter is compared with some existing topologies to validate the performance of the system. The number of power semiconductor switches used in the system is the base factor in this comparison. The number of switching devices used in the particular circuit is an essential factor.

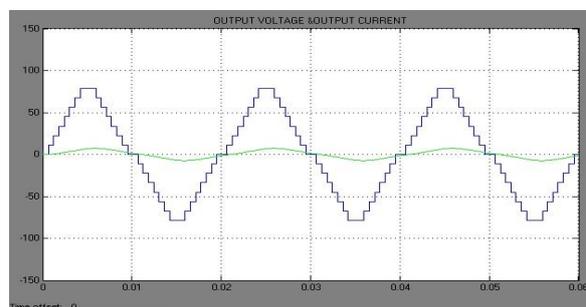


Figure 8. Simulated output voltage and current of proposed 15 level inverter

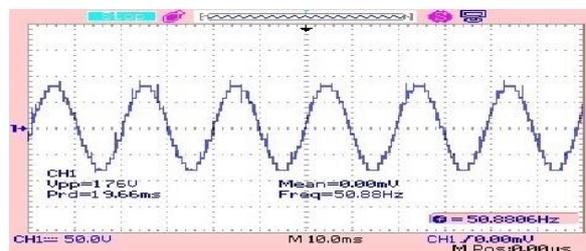


Figure 9. An output voltage of the proposed inverter for R load

Since this factor directly relates to switching losses, driver circuits, size cost effectiveness. The switching losses become reduced if minimum numbers of switches are used for the same level. The driver circuits purely depend on the number of switching devices used, which leads the overall circuit to

become more compact. At the same time, the efficiency of the system also gets increased.

In this work, only 15 levels are presented here. By adding additional cells in the voltage pattern 4, the number of levels can be increased easily. The 31 levels asymmetrical inverter is presented in [13] uses 12 switches and 4 sources, for the same level this proposed system requires only 10 switches and 5 sources. Hence two switches are effectively reduced in the proposed system for the same output level. The system presented in [14] uses 10 switches for the same 15 level. This proposed system uses only 8 switches for the same 15 levels. Similarly, the concept introduced in [15] uses 11 switches for 21 levels. But the proposed scheme uses only 10 switches for 31 levels.

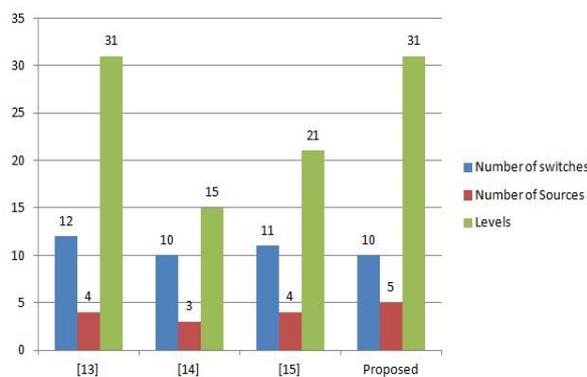


Figure 10. A comparison chart with existing systems

Hence by comparing with these existing schemes, the proposed model uses the minimum number of switches for the same output levels. Thereby this proposed module is more compact than these existing schemes. Hence the switching losses are considerably reduced, and the overall performance gets improved.

6. CONCLUSION

A novel cascaded multilevel inverter without using a full bridge inverter module is proposed here. The two different voltage patterns are described for the proposed scheme. The proposed 11 level and 15 level inverter are simulated, and its results are obtained. The obtained results clearly show the theoretical statements closely relate to the simulated output. This proposed inverter is capable of generating the same output voltage level with the minimum number of switches as compared to the existing schemes. By utilizing the minimum switches, the switching losses can be reduced effectively thereby the efficiency of the system gets improved. The proposed system is validated in both theoretical as well as practical manner.

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