International Journal of Research in Advent Technology, Vol.7, No.5, May 2019
E-ISSN: 2321-9637
Available online at www.ijrat.org

A Review on Non-Conventional Analog Circuit Design Techniques for Low Voltage Low Power Operation

Kiranjeet Kaur[1], Dr. Sandeep Singh Gill[2], Navneet Kaur[3]
Department of Electronics and Communication Engineering[1,3]
Guru Nanak Dev Engineering College,
Ludhiana, Punjab, India
National Institute of Technical Teachers Training and Research[2]
Chandigarh, Punjab, India
Research Scholar[1], Professor[2], Assistant Professor[3]
kiranjeetubhi@gmail.com[1], ssg270870@yahoo.co.in[2], navneetkaur@gndec.ac.in[3]

Abstract- Designing of integrated circuits under low voltage low power condition is becoming an indispensible issue in today's era. Reducing the power consumption and power supply voltage is the key challenge as it makes certain about reliability of device, averts overheating of the circuits and extends the battery for portable electronics, battery powered implantable and wearable medical devices. Small size and light weight devices are in demand in modern span. Various innovative techniques and methods have been suggested and implemented in literature to decrease the power consumption and enhance the speed by changing the base material of the chips from traditional Silicon to III-V material like Gallium Arsenide. Non-conventional techniques have played pivoted role in minimizing the design complexity and drive the power supply voltage towards the threshold voltage of MOS transistors. This paper presents the operation principle, advantages and disadvantages of non-conventional analog circuit design techniques such as Bulk driven technique, Floating gate technique and Quasi Floating gate technique, thus enabling circuit designers to select the proper design technique based on application requirements.

Index Terms- Bulk driven, Floating gate, Quasi floating gate, complementary metal oxide semiconductor (CMOS), low voltage low power (LVLP)

1. INTRODUCTION

The increasing usage of portable devices and the need to reduce power usage has led to an inclination towards development of new techniques to alleviate this problem [1]. Attaining Low voltage Low power operation through a variety of non-conventional analog circuit design techniques has been discussed in this article.

Advanced semiconductor technology (BiCMOS) combine bipolar junction transistor and CMOS transistor in a single IC and merge the benefits of both transistor types. Speed over purely bipolar technology is improved by this technology and provides lesser power dissipation over purely CMOS, high analog performance, and smaller size of IC with high reliability. But this technology involve additional steps of fabrication which raise the process cost [1-2].

Under SOI (Silicon on insulator) technology, by Si oxidation or by oxygen implantation into Si a layer of silicon dioxide is implanted below the surface. Buried oxide (BOX) is termed as the implanted silicon dioxide by which parasitic capacitance is minimized and the performance of the device is enhanced. This technology possesses some advantages such as smaller layout area, ideal device isolation and high speed of switching and lesser power consumption. However, fabrication process of this technology is more costly [1, 3].

- In CMOS technology both p-channel MOSFET and n-channel MOSFET are used in a complementary way on the same substrate. CMOS technology is widely used in the fabrication of conventional microchip because it is less expensive than BiCMOS and SOI technologies and therefore resulting in better performance, high density and lesser power dissipation. The supply voltage is reduced in order to make sure about the device consistency as the MOS transistor dimensions are shrunk. Since devices with higher value of threshold voltage have higher value of noise margin and smaller leakages therefore, the threshold voltage is not scaled down by the same amount [4]. The main drawback in LV LP analog circuit design is high value of the threshold voltage. Many techniques are used to overcome this limitation based on CMOS technology. The threshold voltage is decreased by making use of these techniques [1]. The most commonly used techniques for LV LP analog circuits design are:

- Level shifter technique [3].
- Rail-to-rail operating range circuits [5-6].
- Weak inversion MOSFET [7].
- Bulk driven technique [4, 29, 30, 31, 32, 33, 9, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43].
- Floating gate technique [3, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19].
- Quasi floating gate technique [20, 21, 22, 23, 24, 25, 26, 27, 28].

Non-conventional analog circuit design techniques are Bulk driven, Floating gate, Quasi floating gate technique and they provide benefits such as simplicity in design and ability to work under LV LP condition with sufficient circuit's performances. Circuits based on these techniques are apt for ultra LV LP application as battery-powered implantable and wearable medical devices [1].

2. NON-CONVENTIONAL TECHNIQUES

2.1 Bulk Driven Technique

MOS transistor is having four terminals named as Drain "D", Gate "G", Source "S" and Bulk "B" and its cross section is shown in Fig.1. For P-type MOS transistor, the Bulk terminal "B" is connected to positive supply voltage and for N-type MOS transistor, this terminal is connected to the negative supply voltage, depending on the type of technology used. The bulk terminal "B" is generally neglected and not used as a signal terminal and therefore, many of the applications are unobserved. The fundamental concept of this technique was initially discussed in [1, 32].

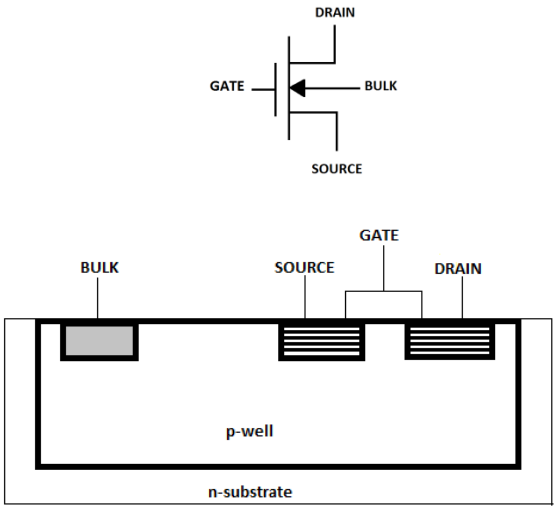

Figure 1.Bulk Driven Technique [1]

In order to form an inversion layer under the gate oxide, the gate-source voltage must be put to a proper bias voltage in this design technique. In the Bulk terminal "B", the input signal is supplied. The working of this design technique is very much similar to that of JFET [1]. Using a positive feedback, the small transconductance of the bulk-driven devices is increased and the noise performance is also improved [44].

The threshold voltage constraint is detached from the path of the signal which enhances the available signal swing due to depletion transfer characteristic of the BD MOS transistor [45].

The polarity of the bulk driven MOS transistor is technology related. This may bound its applications. For example, a dual well process is required to realize rail-to-rail bulk driven op-amp. This process is more costly and larger chip area is needed [46].

2.2 Floating Gate Technique

Nowadays, many innovative and significant LV LP applications have been designed using the floating gate technique [1,10,11,12,13,14,15,16,17,18,19] because of the adjustable threshold voltage. The most important application of the Floating gate analog design technique was to pile up information in digital memories and flash memories [17]. The representation of the Floating gate MOS transistor with two control gates and its analogous circuit is shown in Fig.2. The gate in floating gate MOS transistor is fabricated using the poly1 layer and is left floating. Gin and Gbias are two control gates that are formed using the second poly layer. At the second control gate 'Gin', the input signal is provided and balances the inversion layer and therefore, controlling the drain current.

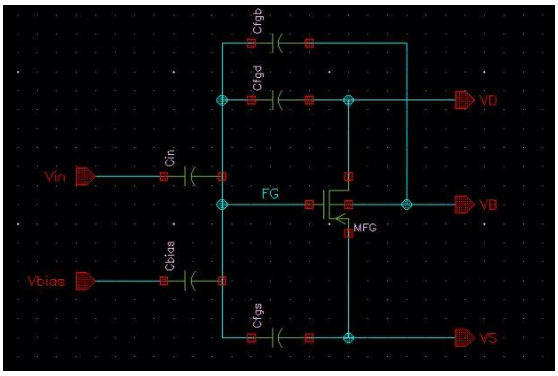

Figure 2.Floating Gate Technique [1]

Floating gate MOS is well-compatible with standard double-poly CMOS process technology and its application in designing Digital to Analog (D/A) and Analog to Digital (A/D) converters [47].

To lower the power dissipation and enhance the system consistency, lowering power supply voltage is the most competent method [48]. To make use of

floating gate MOS transistors for threshold modification in tunable resistor, current mode divider and variable transresistance amplifier is explored [48].The floating gate analog design technique is used to supply operation at low voltage [49]. The Floating gate MOS transistor with multiple inputs can be achieved by the gate electrode which extends over the channel [49].

2.3 Quasi Floating Gate Technique

There are many research articles which describe significant implementations of the Quasi floating gate MOS transistor in Low voltage Low power applications [1, 20, 21, 22, 23, 24, 25, 26, 27, 28]. The Quasi floating gate MOS transistor emerges as an extended form of Floating gate MOS transistor in order to overcome its limitation. The comparatively large bias capacitance value of the Floating gate MOS transistor results in enhancement in the silicon area, effective transconductance and Gain Bandwidth product (GBW) are reduced. Using the Quasi floating gate MOS transistor, there is reduction in the occupied chip area and the initial charge is no longer a bottleneck [8]. Depending on the transistor type, the floating gate is tied through a large value resistor to a proper bias voltage. Fig.3 and Fig.4 shows the equivalent circuit of QFG MOS transistor with single input terminal. Practically, a leakage resistance 'Rlkg' of a diode connected MOS transistor 'MR' is implemented rather than a typical resistor [1].

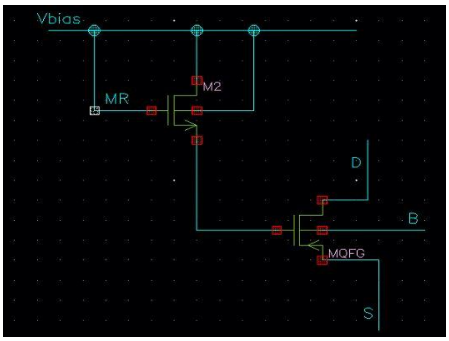

Figure 3.Quasi Floating Gate Technique [1]

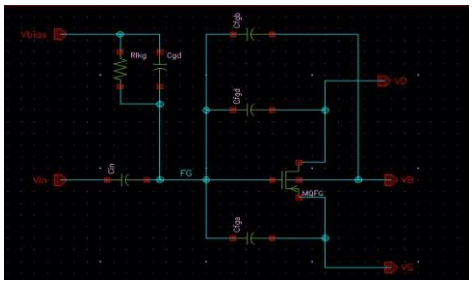

Figure 4.Quasi Floating Gate Technique [1]

Bulk driven, Floating gate, Quasi floating gate are the modern analog circuit design techniques and their compositions are used to solve the high threshold voltage. The input common mode range is increased while maintaining other circuit's performance [50].

The Quasi floating gate MOS transistor and Floating gate MOS transistor both are very similar. There are few differences about DC biasing point between Floating gate and Quasi floating gate. In Floating gate MOS transistor, the DC biasing point for the transistor is left suspended and the gate of Quasi floating gate MOS transistor is not left suspended at DC. Moreover, resistor of large value is connected to the gate terminal "G" and then coupled to power supply. In other words, the gate terminal "G" is attached to V_{DD} (V_{SS}) through a large valued resistor for NMOS (PMOS) transistor. There is another issue about quasi floating gate MOS transistor. It is recognized that fabrication of resistor having large value in CMOS process is not easy and expensive. It will further result to the increase in chip area as well as cost of manufacturing [20].

3. BENEFITS AND LIMITATIONS

3.1 Bulk Driven Technique

Benefits of using the Bulk driven technique are as given below:

- Requirements of threshold voltage are removed [1].
- It is appropriate for the circuits in which the signal swings all the way. It can also be designed by the basic MOSFET [1].
- DC and AC can be processed over the Floating gate and Quasi floating gate processes AC only [1].

Limitations of using the Bulk driven technique are as given below:

- The value of transconductance and transition frequency is small as compared to gate driven technique. Input noise is more [1].
- Twin well process is used when both P-type and N-type MOS transistors are used like Bulk driven MOS transistors and that will increase the process cost and chip area is increased [1].
- Analog circuits having tight matching between Bulk driven MOS transistors are complicated to fabricate because Bulk driven MOS transistors are fabricated in different wells [1].
- Problem of short circuit may occur [1].

3.2 Floating Gate Technique

Advantages of using the floating gate technique are as follows:

- Multi-input terminals are possible. According to the requirements of specific application, threshold voltage can be adjusted [1].
- It is useful in where ultra low voltage and ultra low power operations are performed [1].
- It can be made up in any of the MOS technology and double poly technology is suggested for better performance [1].

Disadvantages of using the floating gate technique are as follows:

- The bias and input capacitances have reasonably large values so more area is taken over the Gate driven MOS transistors. [23, 27].
- In the Floating gate, there is unsure amount of cumulative initial charge [1].
- In comparison with Gate driven MOS transistors, there is reduction in the value of effective transconductance and output impedance [1].
- The transition frequency is small and therefore bandwidth is also small [1].

3.3 Quasi Floating Gate Technique

Pros of quasi floating gate technique are as under:

- At the floating gate, there is no initial charge trapped [1].
- Smaller chip area is occupied [1].
- Effective transconductance is more [1].

Cons of quasi floating gate technique are as under:

- Higher effective output conductance than the effective output conductance of Floating gate MOS transistor and the output conductance of Gate driven MOS transistor [1].
- Floating gate voltage must not go beyond the knee voltage [1].

4. CONCLUSION

Reducing the voltage supply and minimizing the power consumption becomes main concern for portable electronics and devices of battery-powered implantable. This paper presented the principle, benefits and limitations of non-conventional analog circuit design techniques for LVLP analog circuit so that suitable technique can be use for dedicated analog circuit design. These techniques provide some desirable features such as simple design with better output, low voltage low power operation, and few undesirable features such as the lowering of the gain bandwidth product (GBW), output impedance and transconductance (in floating gate and quasi floating gate technique case).

ACKNOWLEDGEMENT

The authors would like to express their obliged thanks to Dr. Sehijpal Singh, Principal of Guru Nanak Dev Engineering College, Ludhiana for offering needed amenities during the course of this paper work.

REFERENCES

[1] Khateb, F., Bay Abo Dabbous, S., Vlassis, S., "A survey of non-conventional techniques for low-voltage, low-power analog circuits design", *Radioengineering*, 2013, 22, pp. 415–427.

[2] Daly, J. C., Galipeau, *D. P.*, "Analog BICMOS Design Practices and Pitfalls", *USA: CRC press LLC*, 2000.

[3] Sakurai, T., Matsuzawa, A., Douseki, T., "Fully-depleted SOI CMOS Circuits and Technology for Ultralow-power Applications", Japan: Springer, 2006.

[4] Rajput, S. S., Jamuar, S. S., "Low voltage analog circuit design techniques*"* IEEE Circuits and Systems Magazine, 2002, vol. 2, no. 1, pp. 24 – 42.

[5] Duque-carrillo, F., Carrillo, J. M., Ausin, J. L., Torelli, G., "Input/output rail-to-rail CMOS operational amplifier with shaped common-mode response", Analog Integrated Circuits and Signal Processing, 2003, vol. 34, no. 3, pp. 221 - 232.

[6] Duque-carrillo, J. F., Carrillo, J. M., Torelli, G., Ausin, J. L., " Common-mode response overlapping vs. shaping in rail-to-rail op-amp input stages", Analog Integrated Circuits and Signal Processing, *2*004, vol. 40, no. 1, pp. 21 - 29.

[7] Vittoz, E. A., "Weak inversion for ultra low power and very low voltage circuits", In Proceedings of Solid State Circuits Conference A-SSCC. 2009, pp. 129 – 132.

[8] Rodriguez-villegas, E, ". Low Power and Low Voltage Circuit Design with the FGMOS Transistor", London: Institution of Engineering and Technology, 2006.

[9] Yan, S., Sanchez-sinencio, E., "Low voltage analog circuit design techniques*:* A tutorial", IEICE Trans. Analog Integrated Circuits and Systems, 2000, vol. E00–A, no. 2

[10] Navarro, I., Lopez-martin, A. J., De la Cruz, C. A., Carlosena, A., "A compact four-quadrant floating-gate MOS multiplier" , Analog Integrated Circuits and Signal Processing, 2004, pp. 159 - 166.

[11] Khateb, F., Khatib, N., Koton, J., "Novel low-voltage ultra low-power DVCC based on floating- gate folded cascode OTA", *Microelectronics* Journal, 2011, pp. 1010 - 1017.

[12] Yin, L., Embai, S. H. K., Sanchez-Sinencio, E., "A floating gate MOSFET D/A converter", In

Proceedings of the IEEE International Symposium on Circuits and Systems, 1997, pp. 409– 412.

[13]Raisanen-ruotsalainen, E., Lasanen, K., Kostamovaara, J., "A 1.2 V micropower CMOS op amp with floating gate input transistors", In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems. 2000, vol. 2, pp. 794 – 797.

[14] Chawla, R., Serrano, G., Allen, D., Hasler, P., "Programmable floating-gate second-order sections for Gm-C filter applications", In Proceedings of the 48th Midwest Symposium on Circuits and Systems. 2005, vol. 2, pp. 1649 - 1652.

[15] Chawla, R., Adil, F., Hasler, P. E., Serrano, G., "Programmable Gm–C filters using floating-gate operational transconductance amplifiers", IEEE Transactions on Circuits and Systems, 2007, pp. 481 - 491.

[16] Babu, V. S., Sekhar, A., Devi, R. S., Baiju, M. R., "Floating gate MOSFET based operational transconductance amplifier and study of mismatch", In Proceedings of the 4th IEEE Conference on Industrial Electronics and Applications. 2009, pp. 127 - 132.

[17] Khateb, F., Khatib, N., Kubánek, D., "Novel ultra-low power class AB CCII+ based on floating-gate folded cascade OTA", Circuits, Systems, and Signal Processing Journal, 2012,vol. 31, no. 2, pp. 447 - 464.

[18] Carvajal, R. G., Torralba, A., Tombs, J., Munoz, F., ramirez-angulo, J., " Low voltage class AB output stage for CMOS op-amps using multiple input floating gate transistors", Analog Integrated Circuits and Signal Processing, 2003, vol. 36, no. 3, pp. 245 – 249.

[19] Lopez-martn, A. J., Ramirez-angulo, J., Carvajal, R. G., Acosta, L., "CMOS transconductors with continuous tuning using FGMOS balanced output current scaling", IEEE Journal of Solid-State Circuits, 2008, vol. 43, no. 5, pp. 1313 - 1323.

[20] Ren, L., Zhu, Z., Yang, Y., "Design of ultra-low voltage op amp based on quasi-floating gate transistors", In Proceedings of the 7th International Solid –State and Integrated Circuits and Technology Conference. 2004, vol. 2, pp. 1465 - 1468.

[21] Ramirez-angulo, J., Urquidi, C., Gonzalez-corvajal, R., Torralba, A., "Sub-volt supply analog circuits based on quasi-floating gate transistors", In Proceedings of the International Symposium on Circuits and Systems ISCAS '03. Bangkok (Thailand), 2003, vol. 1, pp. 781 - 784.

[22] Ramirez-angulo, J., Lopez-Martin, A. J., Carvajal, R. G., Chavero, F. M., "Very low-voltage analog signal processing based on quasi-floating gate transistors", IEEE Journal of Solid-State Circuits, 2004, vol. 39, no. 3, pp. 434 - 442.

[23] Khateb, F., Khatib, N., Kubánek, D., "Low-voltage ultralow-power current conveyor based on quasi-floating gate transistors", *Radioengineering*, 2012, vol. 21, no. 2, pp. 725 - 735.

[24] Gupta, R., Sharma, S., Jamuar, S. S., "A low voltage current mirror based on quasi-floating gate MOSFETs", In IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). 2010, pp. 580 – 583.

[25] Lopez_martin, A. J., Acosta, L., Algueta miguel, J. M., Ramirez-angulo, J., Carvajal, R. G., "Micropower class AB CMOS current conveyor based on quasi-floating gate techniques", *In* Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems. 2009, pp. 140 - 143.

[26] Garcia-alberdi, C., Lopez-martn, A.J., Acosta, L., Carvajal, R. G., Ramirez-Angulo, J., "Class AB CMOS tunable transconductor", In Proceedings of the 53rd IEEE Internat. Midwest Symp. on Circuits and Systems MWSCAS. 2010, pp. 596 - 599.

[27] Algueta miguel, J. M., De la cruz BLAS, C.A., Lopezmartn, A. J., "CMOS triode transconductor based on quasi floating-gate transistors", Electronics Letters, 2010, vol. 46, no. 17, pp. 1190 - 1191.

[28] Algueta miguel, J. M., Lopez-martin, A. J., Acosta, L., Ramirez-angulo, J., Carvajal, R. G., " Using floating gate and quasi-floating gate techniques for rail-to-rail tunable CMOS transconductor design", IEEE Transactions on Circuits and Systems, 2011, vol. 58, no. 7, pp. 1604 - 1614.

[29] Urban, C. S., Moon, J. E., Mukund, P. R., "Designing bulk driven MOSFETs for ultra-low-voltage analogue applications", Semiconductor Science and Technology 2010, vol. 25, pp. 1 - 8.

[30] Khateb, F., Biolek, D., Khatib, N., Vavra, J.,"Utilizing the bulk-driven technique in analog circuit design", In IEEE 13th International Symposium on Design and Diagnostics of Electronic Circuits and Systems. Vienna (Austria), 2010, pp. 16 – 19.

[31] Urban, C. S., Moon, J. E., Mukund, P. R., "Scaling the bulk driven MOSFET into deca-nanometer bulk CMOS processes", Microelectronics Reliability, 2011, vol. 51, no. 4, pp. 727 - 732.

[32] Guzinski, A., Bialko, M., Matheau, J. C., "Body-driven differential amplifier for application in continuous-time active C filter", In Proc. ECCD. Paris (France), 1987, pp. 315 - 319.

[33] Khateb, F., Kacar, F., Khatib, N., Kubánek, D., "High precision differential-input buffered and external transconductance amplifier for low-

voltage low-power applications", Circuits, Systems, and Signal Processing, 2012, vol. 31, pp. 453 - 476.

[34] Carrillo, J. M., Torelli, G., Perez-aloe, R., Duquecarrillo, F., "1-V rail-to-rail bulk-driven CMOS OTA with enhanced gain and gain-bandwidth product", In Proceedings of the European Circuit Theory and Design Conf. 2005, pp. 261 to 264.

[35] Vlassis, S., Raikos, G. Bulk-driven differential voltage follower. Electronics Letters, 2009, vol. 45, pp. 1276 - 1277.

[36] Carrillo, J. M., Torelli, G., Perez-aloe, R., Valverde, J. M., Duque-carrillo, J. F., "Single-pair bulk driven CMOS input stage: A compact low-voltage analog cell for scaled technologies," Integration, the VLSI Journal, 2010, vol. 43, pp. 251 - 257.

[37] Raikos, G., Vlassis, S., Psychalinos, C., "0.5 V bulk driven analog building blocks", International Journal of Electronics and Communication (AEÜ), 2012, vol. 66, pp. 920 - 927.

[38] Khatib, N., Khateb, F., "New bulk-driven DVCC based on folded cascode structure," In Proceeding of Electronic Devices and Systems IMAPS CS International Conference, 2011, pp. 211 - 216.

[39] Raikos, G., Vlassis, S., "0.8V bulk-driven operational amplifier", Analog Integrated Circuits and Signal Processing, 2009, pp. 425 - 432.

[40] Pan, S-W., Chuang, C-C., Yang, C-H., Lai, Y-S, "A novel OTA with dual bulk-driven input stage", In Proc. IEEE Int. Symp. on Circuits and Systems ISCAS. 2009, pp. 2721 - 2724.

[41] Rosenfeld, J., Kozak, M., Friedman, E. G., " A bulk-driven CMOS OTA with 68 dB DC gain", In Proceedings of the 11th IEEE International Conference on Electronics, Circuits and Systems ICECS. 2004, pp. *5 – 8*

[42] Khateb, F., Khatib, N., Kubánek, D., "Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascode OTA", *Microelectron. J.*, 2011, vol. 42, no.5, pp. 622 – 631.

[43] Khateb, F., Biolek, D., "Bulk-driven current differencing transconductance amplifier", Circuits, Systems, and Signal Processing, 2011, pp. 1071 - 1089.

[44] Raikos, G., Vlassis, S. "0.8 V bulk-driven operational amplifier", Analog Integr. Circuits Signal Process, 2010, 63, pp. 425–432.

[45] Kulej, T., Khateb, F. "0.4-V bulk-driven differential-difference amplifier", *Microelectron. J.*, 2015, vol. 46, pp. 362–369.

[46] Khateb, F., Biolek, D., Khatib, N., Vavra, J., "Utilizing the bulk-driven technique in analog circuit design", In IEEE 13th International Symposium on Design and Diagnostics of Electronic Circuits and Systems. Vienna (Austria), 2010, pp. 16 - 19.

[47] Gupta, M., Pandey, R., "Low-voltage FGMOS based analog building blocks", *Microelectron. J.*, 2011, vol. 42, pp. 903–912.

[48] Gupta, M., Pandey, R., "FGMOS based voltage-controlled resistor and its applications", *Microelectron. J.*, 2010, vol. 41, pp. 25–32.

[49] Kumngern, M., Khateb, F., "Fully differential difference transconductance amplifier using FG-MOS transistors" Int. Symp. Intelligent Signal Processing and Communication Systems (ISPACS), 2015, pp. 337–341.

[50] Khateb, F., Kumngern, M., Kulej, T., Kledrowetz, V., "Low-voltage fully differential difference transconductance amplifier", *IET Circuits Devices Syst. J.*, 2018, vol. 12, Iss. 1, pp. 73-8.