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Innovations In Techniques And Design Strategies For Leakage And Overall Power Reduction In Cmos Vlsi Circuits: A Review

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ABSTRACT

The voltage scaling is used as prominent technique to improve energy efficiency in digital systems where it is a vital parameter for power reduction in CMOS VLSI design and more often than not these can be related with leakage current and its reduction in various ways, however it is not the only technique capable of doing so. Scale reduce the effects of supply voltage on the quadratic reduction of energy Consumption of the system. There are methods where supply voltage inductor reduction time errors in the system can be corrected by error detection and correction circuits. In this work we review various power reduction techniques where voltage between focused operators based on scales applications that can tolerate errors with the entire system can be designed with justification. It has the ability to characterize the basic Arithmetic operators that use different operation strategies (combination supply voltage supply, body polarization scheme and clock frequency) generate models for the operators addressed. error file Applications can be mapped with the approximate approximation operator models to achieve optimal deviation between energy effectiveness and margin of error. This paper looks to find and provide briefings of some of the techniques that has been proposed in order to reduce leakage current and provide low power VLSI systems.

Keywords—Leakage current; CMOS VLSI;Voltage Scaling; Sleeper and Stack.

I. INTRODUCTION

The design procedures of low powered devices are one of the major advances the world has seen in the recent years as far as the electronic industry goes. When it comes to VLSI circuits, the most important aspect of the design parameter is associated with the phenomenon of power dissipation. It is this particular parameter which influences many a device and their effectiveness specially when they are battery operated. With the constant demand of an ever increasing thirst for chip density opposed by a constant demand of ever decreasing chip size are two of the major hindrances in being able to design systems which are higher powered while being small in size.It can also be stated that below 100 nm mode, the possibilities of power management is becoming more and more difficult because of the increased complexity of design it is associated with.Apart from this leakage current also plays a vital role in relation to power management in low power VLSI devices.In sub-micron technologies, leakage and dynamic power consumption is becoming an essential design parameter as it is dissipating a considerable portion of the total power consumption. [1].Voltage scaling is another approach that can be utilized for applications in energy-harvested systems [6] .

II. VARIOUS LOW POWER STRATEGIES

The following (table-1) shows some different strategies available at different level in VLSI design process for optimizing the power consumption:

Design	Employed Strategy
Level related to circuit or logic	Sizing of transistor and energy recovery

Level related to Architecture	Various encoding schemes ,pipelining strategies
Level related to Software	Strategy related to locality and concurrency
Level related to Technology	Reduction of threshold values, supporting multiple threshold distribution
Level related to Operating System	Dividing in portions and power down solutions

Table 1: Strategies for low power design

III. POWER DISSIPATION BASICS

In a circuit three components are responsible for power dissipation: dynamic power, short-circuit power and static power. Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below [3].

$P_{dyn} = C_L V_{dd}^2 \alpha f$-------- (i)

Where C_L : Load Capacitance, a function of fan-out, wire length, and transistor size, Vdd: Supply Voltage, which has been dropping with successive process nodes, α: Activity Factor, meaning how often, on average, the wires and switch, f :Clock Frequency, which keeps increasing at each successive process node. Static power or leakage power is a function of the supply voltage (Vdd), the switching threshold (Vt), and transistor sizes. As process hubs shrink, leakage turns into a huger wellspring of vitality utilize, expending no less than 30% of aggregate power, Leakage or static power is the power consumed by a device due to transistor leakage and it is produced by the reverse biased current is shown in Fig.1. [4]

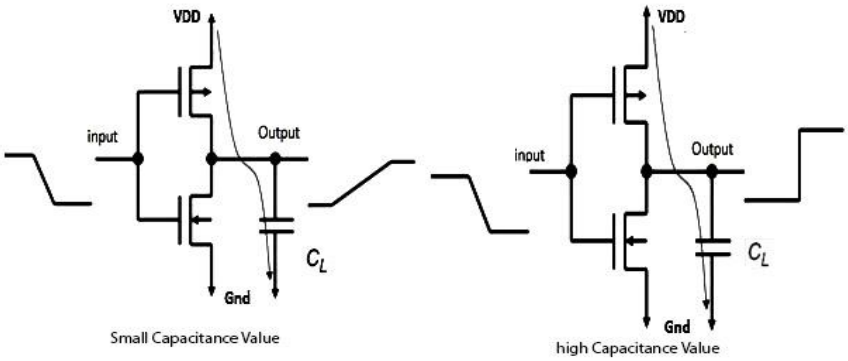

Fig. 1-Leakage power dissipation due to low and high load capacitance

If we think about a technology that comes under deep submicron, leakage power parameter becomes a very important aspect of it, When the CMOS device is operated in both static and switching mode, it is generated. One of the major problem areas of power dissipation is when power is consumed and eventually wasted when the device is in idle state and actually needs no power.[7]

IV. VARIOUS TECHNIQUES

Many researchers as well research groups have developed power models for reducing static power consumption for embedded devices. Power gating [8, 11] is slowly becoming a very popular design technique for decreasing leakage currents.Parallelism and pipelining techniques for power reduction were first proposed by [19]. Since then researchers have conducted studies aimed at optimizing the pipelining depth for dissipated power reduction in CMOS devices. Furthermore, researches have been conducted at a functional block level to compare the performances of pipelining and parallelism to find out which technique performs best when it comes to minimizing total switching power. [9] It was shown that leakage current (source of static power consumption) is a combination of sub threshold and gate-oxide leakage which is

$$I_{leak} = I_{subk} + I_{ax} \text{ -------- (i)}$$

A. Circuit Technique

Here, the authors have used two extra transistors labeled PM2 (PMOS) and NM2 (NMOS) for the purpose of raising the voltage at the source terminal of the MOSFET. Transistor PM2 is configured to work in "cut off" mode (source and gate connected) while the transistor NM2 follows the circuit input conditions. The transistor PM2 is connected between the output node of the circuit and the source terminal of the transistor NM1. The purpose of the transistor PM2 is to supply the leakage currents to the source terminal of the upper NMOS transistor (NM1) to charge the node (source terminal of NM1). During the logic '0' condition at the input, the two NMOS transistors NM1 and NM2 turned off and a logic '1' appears at the output node. As the extra PMOS transistor PM2 set to "cut off" state, it supplies leakage currents and establishes a certain voltage at the source terminal of the upper NMOS transistor NM2 depending on the amount of leakage current provided by the transistor PM2. [5] The increased source voltage (V S) of the upper NMOS transistor (NM1) reduces the drain-to-source voltage (V DS) of the transistor NM1 and then the subthreshold leakage current. The dependency of node voltage on the width of PMOS transistor PM2 is depicted in Fig. 2.

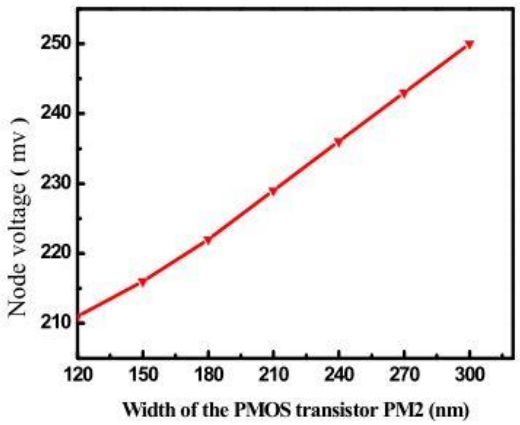

Fig2 : Dependency of node voltage (source terminal of NM1) on the width [5]

B. Leakage Minimization by Input Vector Control

By applying a MLV to a circuit, it is possible to decrease the leakage current of the circuit when it is in the standby mode. Note that applying MLV for leakage reduction is independent of the source of leakage, which may include the subthresholdand the gate tunneling leakage currents. For our experimental results, authors have used SPICE to measure the leakage current of different gates under various input combinations. SPICE simulator reports a leakage current value that includes both the sub- threshold leakage and the gate leakage currents. [2]

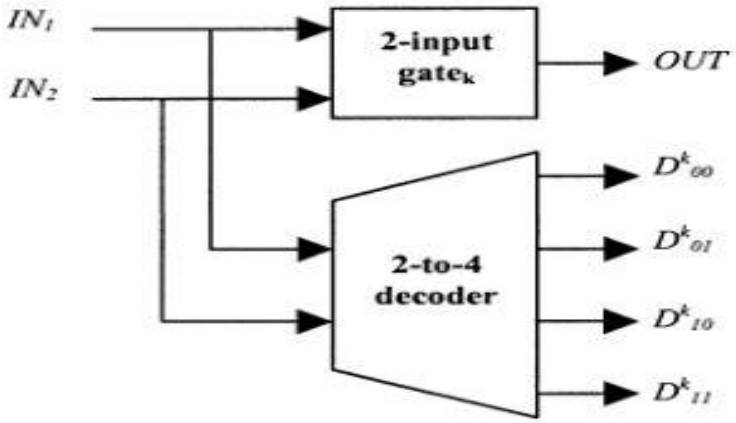

Fig 3 : A 2-to-4 decoder indicating input combinations of a 2-input logic gate [2]

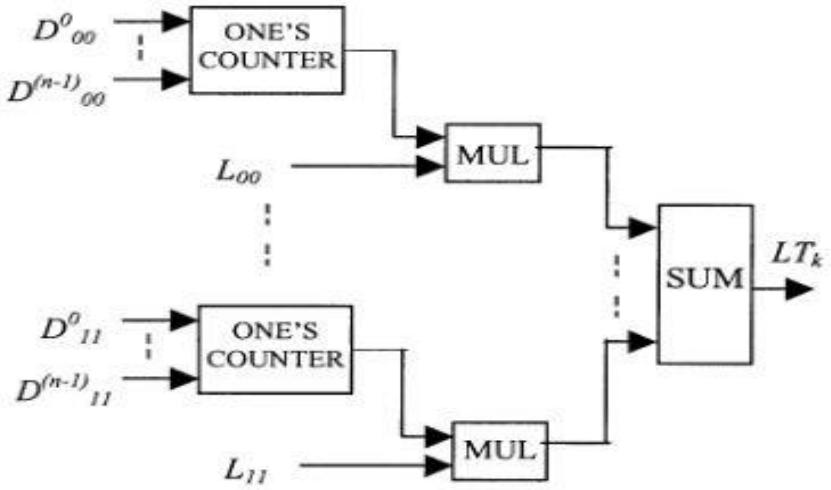

Fig 4 : Contribution of all gates of type k to the total leakage [2]

C. LFS & Sleep Stack With Keeper

In this section, leakage reduction techniques in which the term used is for the first one "leakage feedback with stack (LFS)" approach is implemented and in the and other it is "sleep-stack with keeper". This section explains the structure of the leakage feedback with stack approach and sleep-stack with keeper.

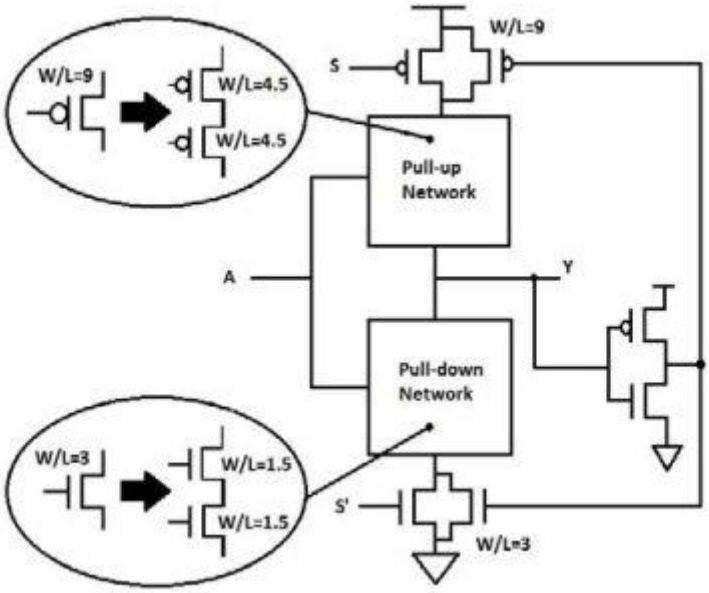

Fig 5 : Leakage feedback with Stack [10]

In first technique i.e. leakage feedback with stack, we are combining the two low power techniques or taking advantage of two techniques i.e. leakage feedback approach due to less transistor than sleepy-stack in which we replaces each transistor in base case into three transistors, and ultra low power technique i.e. Stack approach. This is shown in fig. 5.

In second approach i.e. sleep-stack with keeper, we are combining the three different low power leakage reduction techniques i.e. sleep transistors, stack approach with keeper as shown in fig 6.

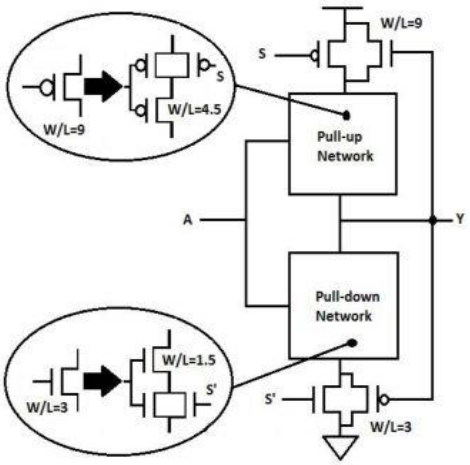

Fig 6 : Sleep stack with keeper approach [10]

V. CONCLUSION

Fast arithmetic cells, including adders and multipliers, are the most used circuits and most of them in many large-scale integration systems (VLSI). The semiconductor industry has experienced explosive growth in the integration of sophisticated multimedia applications into mobile electronic devices over the past decade. The above work by various authors that have been reviewed in this paper explains the need for low power VLSI circuits and presents various design techniques currently in the microelectronics industry. This paper will help designers understand the basic principles of low power as well as motivate them to go for further

implementations already existing in the field. The general description of the various methods has been briefly explained and further work and improvements will be sought in the future.

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