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LOW POWER FULL ADDER WITH REDUCED TRANSISTORS IN EX-OR GATE

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ABSTARCT:
This paper presents as low power efficient full adder with minimized number of transistors. All the DSP processors consists of adder circuits. The power consumption in a full adder circuit is majorly due to EX-OR gates. In this paper a novel EX-OR gate is proposed with only two transistors. This full adder utilizes only six transistors which consume 33.3% less power when compared to eight transistor full adder which was designed earlier. Simulation results were observed using MICROWIND tool.

Keywords: *Low power full adder; power consumption; EX-OR gate.*

1. INTRODUCTION

Achieving low power and reduction in area has become a challenging task in the field of VLSI design. Adders are not only used for arithmetic operation but also necessary to compute virtual physical address in memory fetch operation in all modern computers. Also the adders occupies critical path in key areas of microprocessor, fast adders are prime requirement for the design of fast processing digital system. Many fast adders are available but the design of high speed with low power and less area adders are still challenging. The performance of an arithmetic circuit is found directly subject to all the FAs employed, stimulating the development of a wide variety of FAs for various applications, smaller number of transistors are adopted to achieve the aim of chip area reduction, but the accompanying disadvantages are threshold voltage loss, a low noise margin and a low-output driving capability.

Adders plays significant role in DSP processors because they are its major functional units and all computations of DSP processor are based on full adder. A conventional full adder requires a total of twenty eight transistors. Shubhajit Roy proposed a three transistor EX-OR gate with which a full adder can be constructed with a total of eight transistors by rearranging the Boolean functions of sum and carry. In this paper a novel full adder with six transistors is built using EX-OR gate which requires only two transistors.

2. PREVIOUS WORK

Basic full adder logic circuit shown in below Figure 1 consists of two EX-OR gates, three AND gates and one OR gate. The Boolean equations for sum and carry are given below for the respective logic circuit.

According to the Shubhajit Roy's proposed eight transistor full adder, the Boolean equations are rearranged in such a way that the full adder logic circuit was constructed using two EX-OR gates where each consists of only three transistors. In this three transistor EX-OR gate which is shown in figure 2 when B input is logic '1' the inverter operates like a normal CMOS inverter and when B is at logic '0' , output goes to high impedance state but since the transistor M2 turns ON and acts like a pass transistor which gives 'A' at its output. Thus the EX-OR gate operation is achieved.

Rearranged Boolean equations for eight transistor full adder are given below

Sum = (aΘb)Θcin

Carry=cin.(aΘb) + a.b

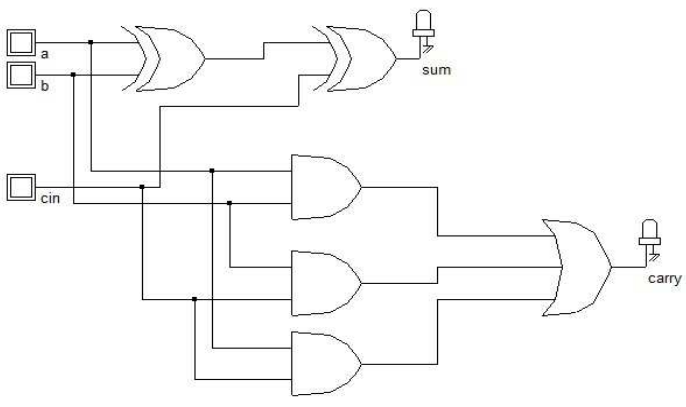

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Figure 1. Full adder logic circuit

Table 1. Truth table of full adder logic circuit

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

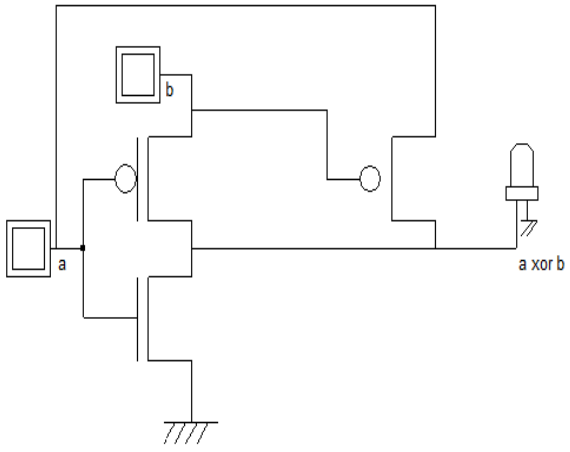

Figure 2. Three Transistor EX-OR gate

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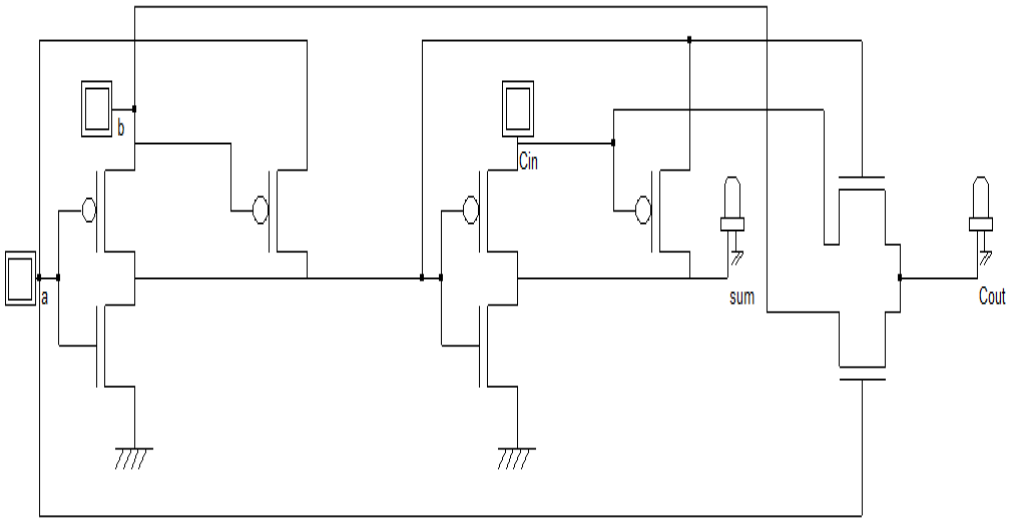

Figure 3. Eight Transistor Full adder

3. PROPOSED WORK

The proposed two transistors EX-OR gate for full adder is constructed by rearranging the Boolean equations for Sum and Carry outputs. The Boolean equations are given below:

Sum = (aΘb).c'+ (aΘb)'.c
Carry= (aΘb)'.a + (aΘb).c

In this proposed design one 2T EX-OR gate drives two 2T EX-OR gates whose outputs are sum and carry. The sum is achieved driving the output of first EX-OR gate module to the gate input of other EX-OR gate module which is consisting of two transistors whose drains are driven 'c'' and 'c' respectively. Similarly Carry is obtained by driving the output of first EX-OR gate module to the gate input of other EX-OR gate module which is consisting of two transistors whose drains are driven by 'a' and 'c'. Finally the full adder is being constructed using only six transistors which occupies less area and consumes less power. The logic circuit for the two transistors EX-OR gate and six transistors full adder are shown in below figures (Figure 3 and Figure 4).

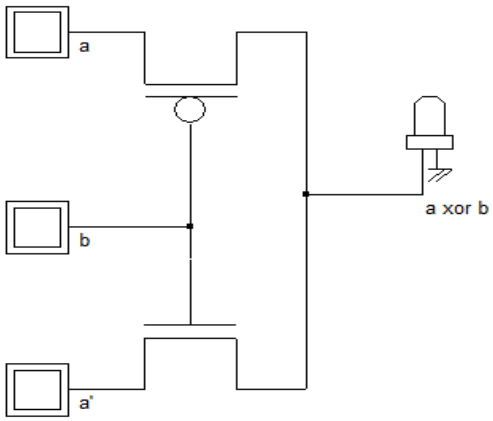

Figure 4. Two Transistor EX-OR gate

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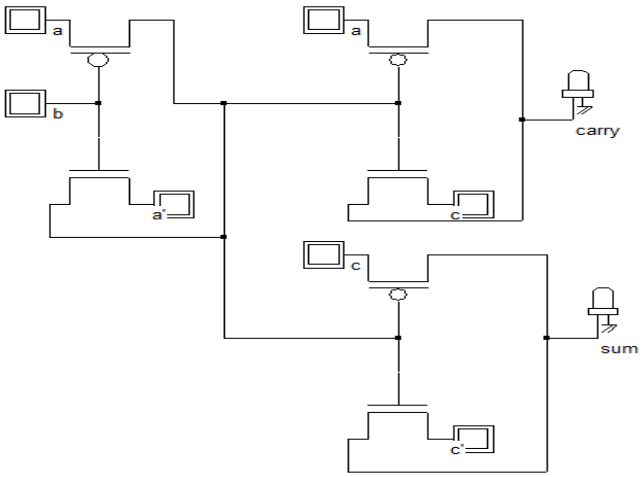

Figure 5. Six Transistors Full adder

4. SIMULATION RESULTS

The proposed design is compared with Shubhajit Roy's full adder circuit and found that the proposed design is area and power efficient. The simulation is being performed on 180nm technology using MICROWIND tool and results were generated for the two designs and area and power consumed were calculated. The comparison results are shown in below table II.

Table II. Comparision results of eight and six transistors full adder

	Previous design	Proposed design
No. of transistors	8	6
Power consumption (µW)	16.8	0.17
Power*delay (µW.nS)	8.9	1.35

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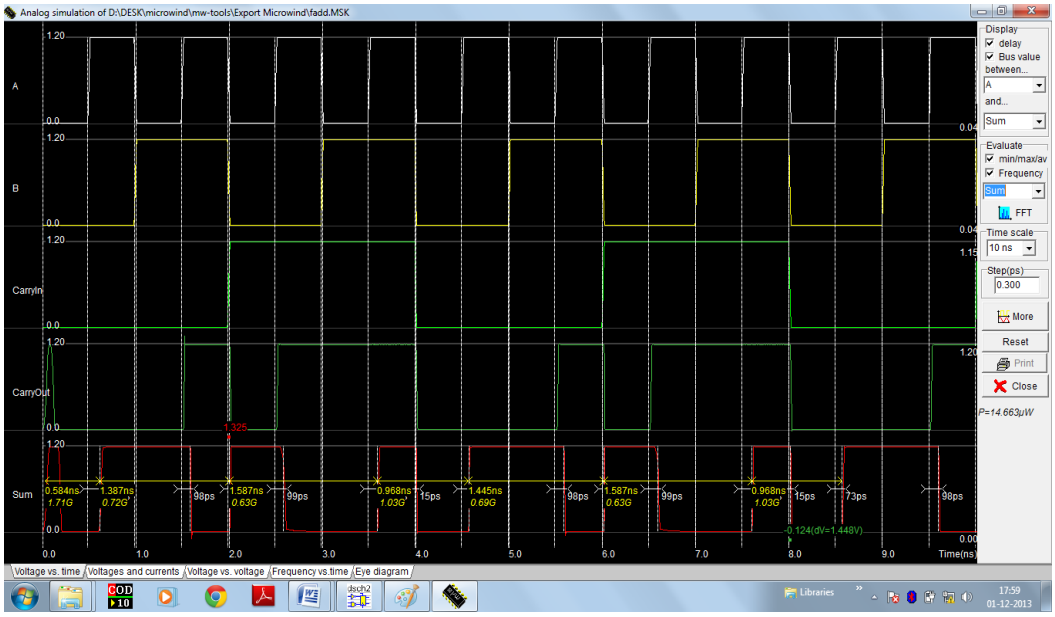

Figure 6 . Simulation result of eight transistor Full adder

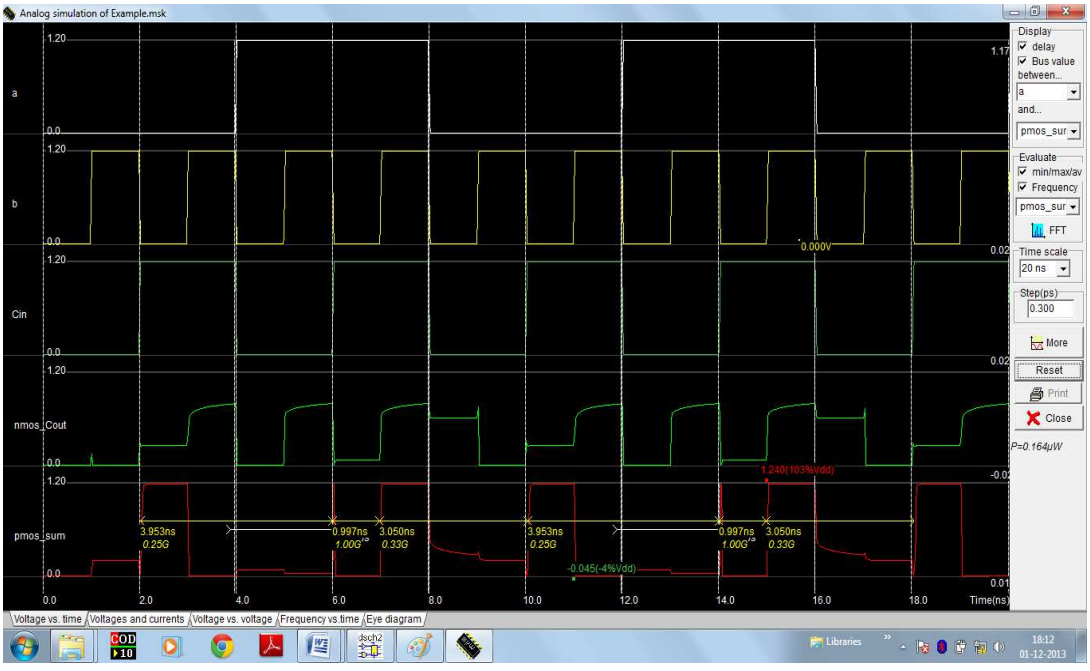

Figure 7. Simulation result of six transistor Full adder

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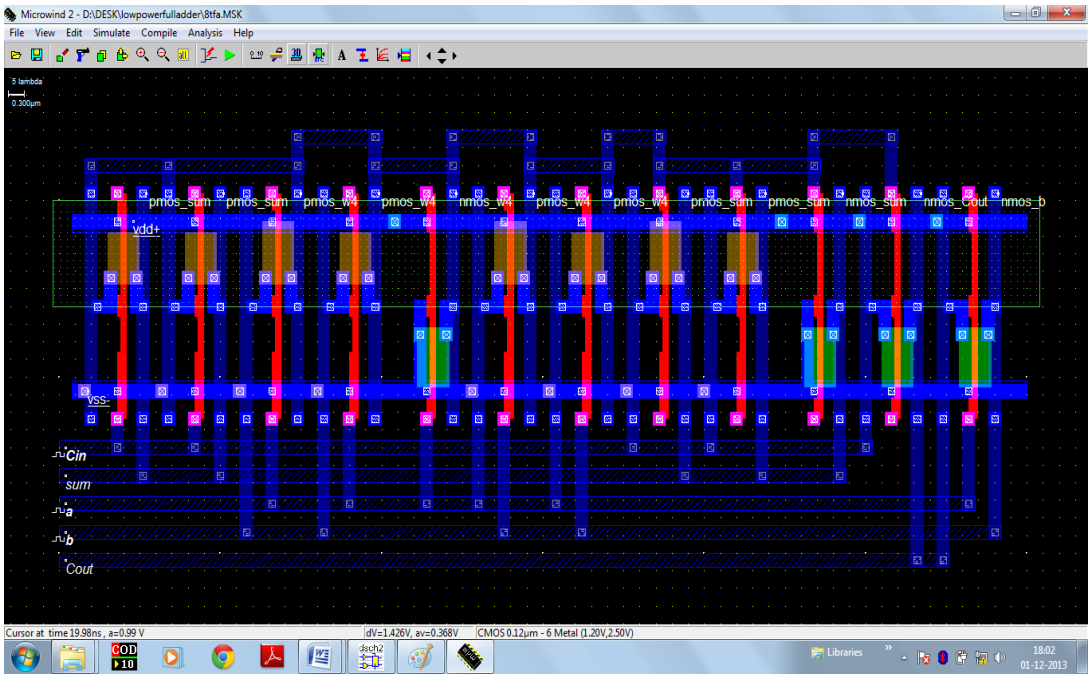

Figure 8. Layout of the eight transistor Full adder

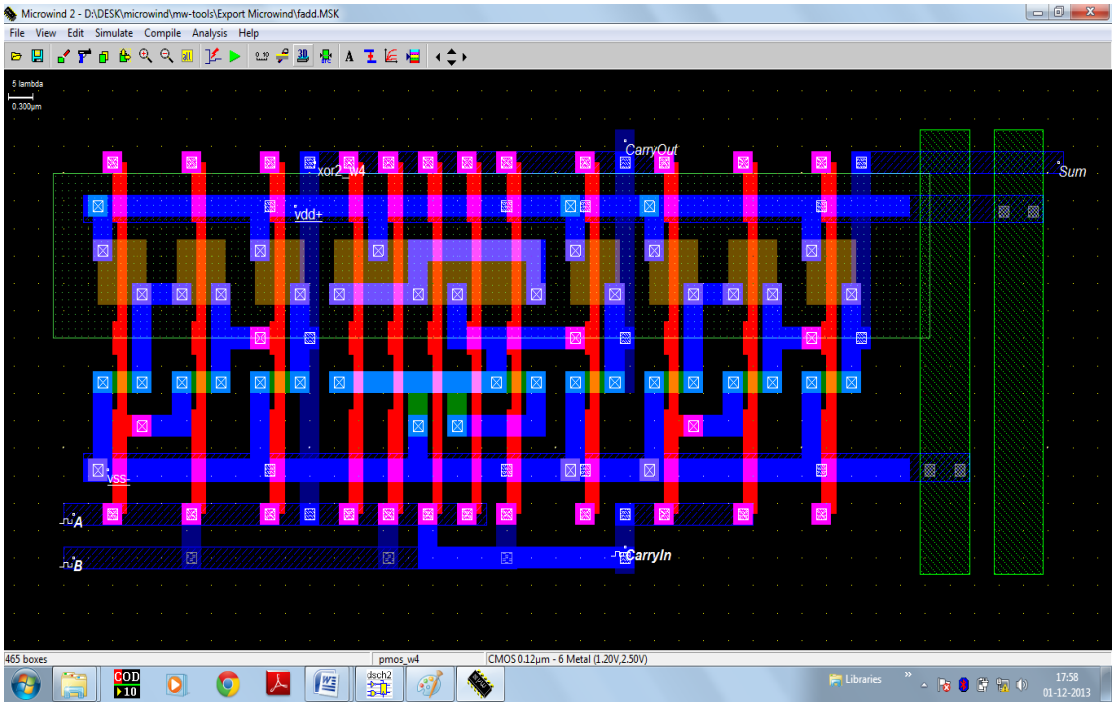

Figure 9. Layout of the Six transistor Full adder

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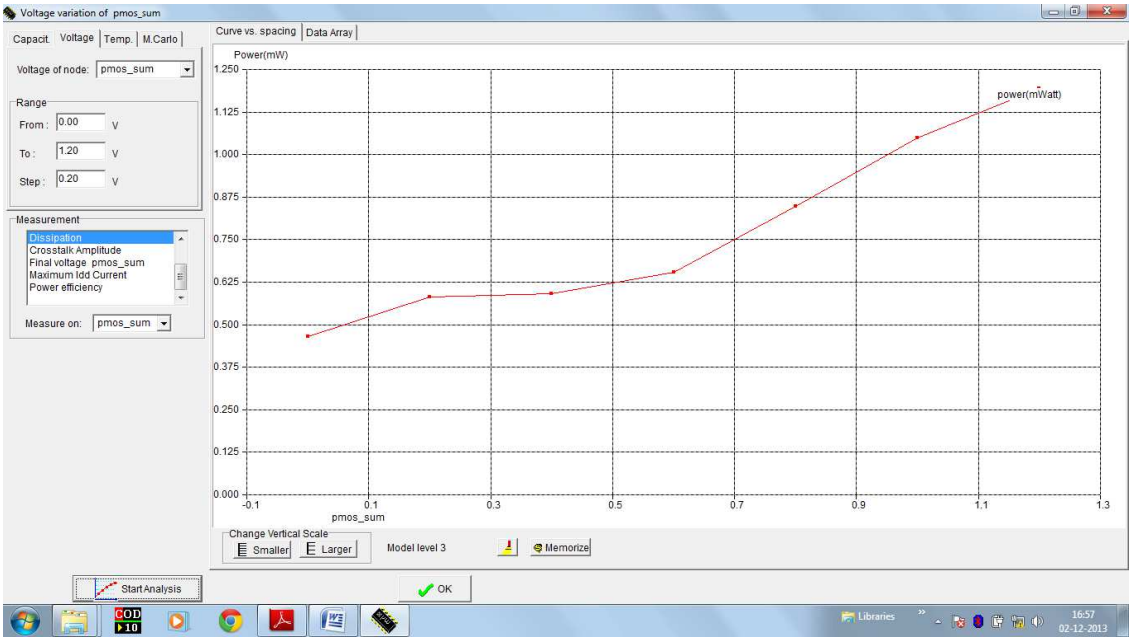

Figure 10.Voltage variation at Sum

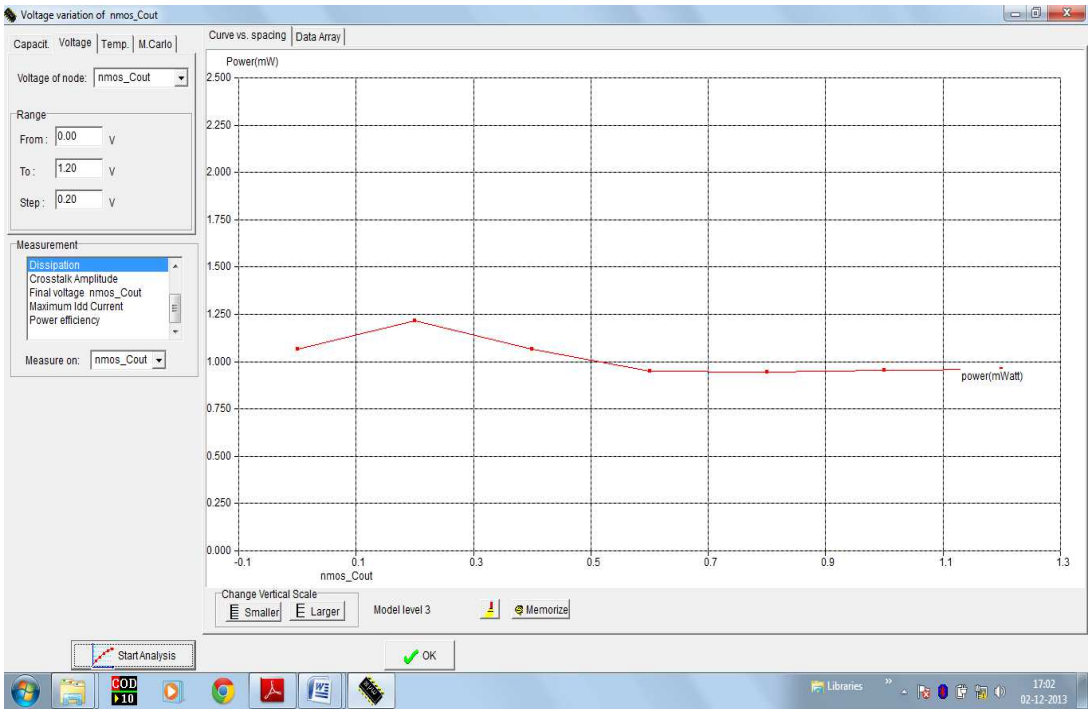

Figure 11.Voltage variation at Carry

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CONCLUSION

The proposed full adder requires six transistors and consumes 0.17µW power and occupies less area than its previous designs. The results were obtained using MICROWIND tool and simulation was done using 180nm technology. Hence the proposed full adder works for low power DSP processor applications.

REFERENCES

[1] Shubhajit Roy Chowdhury, Aritra Banerjee, Aniruddha Roy, Hiranmay Saha "A high Speed 8 Transistor Full Adder Design using Novel 3 Transistor XOR Gates", International Journal of Electrical and Computer Engineering 3:12 2008

[2] Massimo Alioto and Gaetano Palumbo "Analysis and Comparison on Full Adder Block in Submicron Technology" IEEE transactions on very large scale integration (VLSI) systems, vol. 10, no. 6, December 2002 pp 806-823.

[3] N Weste and K. Eshraghian, Principles of CMOS VLSI Design (A Systems Perspective).

[4] E.Abu-Shama and M. Bayoumi, "A new cell for low power adders," in *Proc. Int. Midwest Symp. Circuits Syst.*, 1995, pp. 1014–1017.

[5] K.Chu and D. Pulfrey, "A comparison of CMOS circuit techniques: Differential cascode voltage switch logic versus conventional logic," IEEE J. Solid-State Circuits, vol. SC-22, pp. 528-532, Aug. 1987.

[6] S.Goel, A. Kumar, and M. A.Bayoumi, "Design of robust, energy-efficient full adders for deepsubmicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp.1309–1321, Dec. 2006.

[7] J.F. Lin, Y.T. Hwang, M.-H. Sheu and C.-C. Ho, "A novel high speed and energy efficient 10-transistor full adder design," IEEE Trans. Circuits Syst. I, vol. 54, no. 5, pp. 1050–1059, May 2007.

[8] S. Timarchi, K. Navi, (2009) "Arithmetic Circuits of Redundant SUT-RNS", IEEE Trans. Instrum.Meas, vol. 58, no. 9, pp.2959-2968.

[9] Y. Jiang, A. Al-Sheraidah, Y. Wang, E. Sha and J.G. Chung, (2004) "A novel multiplexer-based lowpower full adder," IEEE Trans. on Circuits and Systems – II: Express Briefs, vol. 51, no. 7, pp. 345-348.

[10] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology," 978-1-4244-2800-7/09/$25.00 ©2009 IEEE

[11] Yi WEI, Ji-zhong SHEN, "Design of a novel low power 8-transistor 1-bit full adder cell," Wei et al. / 604 J Zhejiang Univ-Sci C (Comput & Electron) 2011 12(7):604-607.

[12]] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, July 1997, pp.1079–90.

[13] Low Power Group. Electrical and Computer Engineering Department,CarnegieMellonUniversity. http://www.ece.cmu.edu/lowpower/benchmarks.html

[14] Chandrakasan, I. Yang, C. Vieri, and D. Antoniadis. Design Considerations and tools for Low-Voltage digital system design. In Proceedings of the 33rd ACM/IEEE Design Automation Conference, 1996, pp. 728-733.

[15] C. Hu. Device and Technology Impact on Low Power Electronics. In Low Power Design Methodologies, Kluwer Academic, Boston, pp. 21-36, 1996.

[16] Bui, H.T., Y. Wang and Y. Jiang, 2002. Design and analysis of low power 10-transistor full adders using novel XOR-XNOR gates. IEEE T. Circuits II, 49(1): 25-30.

[17] Reaz, M.B.I. and L.S. Wei, 2004. Adaptive linear neural network filter for fetal ECG extraction. Proceedings of the International Conference on Intelligent Sensing and Information Processing (ICISIP). Chennai, India, Jan. 4-7, pp: 321-324.

[18] Rangaraju, H.G., U. Venugopal, K.N. Muralidhara and K.B. Raja, 2010. Low power reversible parallel binary adder/subtractor. Int. J. VLSI Design Comm. Syst., 1(3): 23-34.

[19] Weste, N. and D. Harris, 2010. CMOS VLSI Design Circuits and Systems Perspective. 4th Edn., Addision Wesley, Boston.

[20] Shalem, R., E. John and L.K. John, 1999. A novel low power energy recovery full adder cell. Proceedings of the 9th Great Lakes Symposium on VLSI. Ann. Abor, MI, USA, Mar. 4-6, pp: 380-383.

[21] Sinha, D., T. Sharma, K.G. Sharm and B.P. Singh, 2011. Design and analysis of low power 1-bit full adder cell. Proceedings of the 3rd International Conference on Electronics Computer Technology. Kanyakumari, India, Apr. 8-10, pp: 303-305.

[22] S.G.Narendra and A.Chandrakasan , Leakage in nanometer CMOS technologies .New York: springer – verlag, 2006.

[23] Jan M.Rabaey , Anantha Chandrakasan and Borioje Nikolic, "Digital Integrated Circuits- Adesign Perspective ", 2nd ed., Prentice Hall of India Pvt Ltd , New Delhi,2006.

[24] N.Weste and K.Eshraghian , "principles of CMOS digital design ," MA :Addisonn Wesley, p.304-307.2005.

[25] Kanika kaur, Arti Noor. POWER ESTIMATION ANALYSIS FOR CMOS CELL STRUCTURES, International Journal of advance Engineering and Technology, Vol 3, issue2, May2012,pp 293-301