An Efficient Implementation of Linear-Phase FIR Filters for Rational Sampling Rate Conversion

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Abstract-In this paper, an efficient technique to implement rational sampling rate conversion (SRC) by a factor of L/M, where L is up-sampling factor and M is down-sampling factor is discussed. In this implementation, the coefficient symmetry of the linear phase finite impulse response filter is exploited as much as possible. This is done in order to reduce the overall implementation complexity (addition as well as multiplication) by using the symmetric FIR filter. The proposed technique is compared to conventional polyphase implementation and fast cyclic convolution algorithms. Overall performance is improved in the proposed technique.

Index Terms – Sampling rate conversion; Finite Impulse Response Filter; Multirate Systems

1. INTRODUCTION

The increasing need of processing digital data at more than one sampling frequency has resulted in the development of a new area of digital signal processing known as multirate signal processing. The basic operations in multirate signal processing are decimation and interpolation. Decimation reduces the sampling rate effectively by compressing the data and retaining the desired information. Interpolation increases the sampling rate. Sampling rate conversion can be done either in analog domain or in digital domain. In the first method, the digital signal is passed through a digital-to analog converter (DAC) and then the analog signal is resampled at the desired rate. In the second method, the resampling of digital data at the desired rate is carried in the digital domain itself.

Sampling rate conversion is the process of converting sampling rate of a signal from one rate to another. This technique is used in many applications like digital audio, communication systems, speech processing, radar systems, antenna systems etc. Sampling rates can be changed upward or downward. Increasing the sampling rate is called interpolation and decreasing the sampling rate is called decimation. The multirate techniques are used to convert the given sampling rate to desired sampling rate and are called multirate system. The basic building blocks of multirate system are interpolators and decimator. Combining these two blocks result in a system that changes the sampling rate by a rational factor L/M. The block diagram of rational sampling rate converter is as shown in Fig.1.
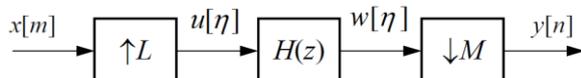

Fig. 1. Rational sampling-rate converter by factor L/M

Robert Bregovic [1] have proposed a method for implementing a linear-phase prototype filter building a nearly perfect reconstruction cosine-modulated FB in such a way that it enables one to partially utilize the coefficient symmetry, thereby reducing the number of required multiplications in the implementation. The proposed method can be applied for implementing FBs with an arbitrary filter order and number of channels. In this paper, an implementation method that reduces the number of required multiplications when implementing a linear-phase prototype filter of an arbitrary order used for building an NPR cosine-modulated FB has been proposed.

Muhammad Ali Siddiqi, Nabeel Samad [2] have presented a practical implementation of multi-stage sample rate conversion in multi-standard software radios. This work includes complete design and subsequent implementation of sample rate conversion filters on a Xilinx Vertex II Pro FPGA Board. A high-level design methodology has been adopted that involves direct HDL code generation from algorithm description for testing and implementation on the FPGA. The prime focus of this paper is the hardware implementation and analysis of the above mentioned architecture. The design has been implemented and tested using ModelSim SE 6.5 and Xilinx ISE Project Navigator, with top level simulations being done in MATLAB. The architecture has been captured using VHDL. Since power consumption is one of the most important parameter in software radio design, the power dissipation measurement of the proposed scheme is compared with an ASIC implementation of two-stage decimation filter in a wireless transceiver. The proposed scheme has been realized onto a Vertex II Pro FPGA using a design methodology which is flexible and allowsthe design and simulation to take place in one step.

Robert Bregovic in [3] has proposed an efficient structure for implementing a linear-phase finite-impulse-response (FIR) filter of an arbitrary order N for the sampling-rate conversion by a rational factor of L/M, where L(M) is the integer up sampling (down sampling) factor to be performed before (after) the actual filter. In this implementation, the coefficient symmetry of the linear-phase filter is exploited as much as possible and the number of delay elements is kept as low as possible while utilizing the following facts. When increasing (decreasing) the sampling rate by a factor of L(M) , only every Lth input sample has a nonzero value (only every Mth output sample has to be evaluated). In this way, the number of required multiplications per output sample is reduced approximately by a factor of two compared with the conventional polyphase implementation.

Yu Huijun [4] has proposed novel design of sampling rate converter based on least square method. To improve the accuracy of signal resampling, a resampling realization method is proposed in this paper. It converts a resampling problem into a time-variable filter designing, so the least square method can be used to obtain the filter coefficients and obtain better accuracy. The experimental results proved that high accuracy signal resampling can be realized with the proposed method. There are two main ways to convert sample rate of a discrete-time system. One is based on polynomial approximation. Although this method has the advantage of high accuracy, the disadvantage is that it has high computation cost. Another is based on multi-rate techniques. This method has the advantage of low computing cost, but the disadvantage is that the filter designing is difficult. A new design of sample-rate converter based on least-square method is proposed to improve the resampling accuracy. To avoid the ill-conditioning problem which may arise in solving the least-square equations, QR decomposition based on householder transformation is used. This resampling method can obtain higher accuracy and easy be implemented. Further work will improve the algorithm to decrease the computation cost.

Dr S. Ramachanderan and Dr B.S. Nagabushan [5] have proposed a novel architecture for sampling rate converter of the demodulator for processing satellite data communication. The overall receiver algorithm is divided into two parts: one to be implemented on an FPGA and the other on a DSP processor. A new distributed arithmetic based architecture for implementing a Sampling Rate Converter is also proposed. The main advantage of this architecture is that it does not employ any MAC unit, whose operational speed is, generally, a bottleneck for high filter throughput. Instead, it makes extensive use of LUTs and hence is ideally suited for FPGA implementation. The main design goals in this work were to maintain low system complexity and reduce power consumption and chip area requirements. The design of a new distributed arithmetic based architecture for sampling rate converter is presented. The main advantage of this architecture is that it does not employ any MAC unit, whose operational speed is, generally, a bottleneck in filter throughput. It makes extensive use of LUTs and hence, is ideally suited for FPGA implementation.

Efficient implementation of such rational SRC have also been presented in many recent works [6][7]. This paper presents an efficient design of rational sampling rate converter by a factor L/M as shown in Fig. 1. based on coefficient symmetry. Section II develops a mathematical model of model shown in Fig. 1. in both time-domain and matrix form. Also, the properties of coefficient matrix are discussed. Section III presents a design example for the proposed technique. Section IV concludes this paper.

2. MATHEMATICAL MODEL FOR RATIONAL SRC

In this section, a complete mathematical analysis of the system shown in Fig. 1 is presented. These relations are used in forthcoming sections for generating an implementation structure for rational sampling rate converter. In this section, first, time domain input output relations for the system are presented. Next, a compact matrix representation for the input output relations is developed.

2.1. *Time Domain Relations*

For the sampling rate converter shown in Fig. 1, the time domain relations are given as

$$u[n] = \begin{cases} x\left[\dfrac{n}{L}\right] & for \ n = 0, L, 2L, \ldots \\ 0 & otherwise \end{cases} \quad (1)$$

$$w[n] = \sum_{k=0}^{N} h_k u[n-k] \quad (2)$$

$$y[n] = w[Mn] \quad (3)$$

where h_k are the coefficients of the transfer function $H(z)$.

The relation between the output sampling rate, denoted by f_{out}, and the input sampling rate, denoted by f_{in}, for the system is given by:

$$f_{out} = \left(\frac{L}{M}\right) f_{in} \quad (4)$$

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The relationship between $u[n]$ and $y[n]$ is given by the following equation:

$$y[n] = \sum_{k=0}^{N} h_k x \left[\frac{Mn-k}{L} \right] \qquad (5)$$

2.2. Matrix Based Relations

The expression in (5) may be considered for $(n + KL)^{th}$ output sample, to represent input-output relations in matrix form from equation (6) to (8).
For the rational sampling rate converter shown in Fig. 1 with rational factor L/M and a filter order N, L consecutive output samples, y[n + l] can be expressed by rewriting expression (8) as shown in (9).

$$y[n + KL] = \sum_{k=0}^{N} h_k x \left[\frac{M(n+KL)-k}{L} \right] = \sum_{k=0}^{N} h_k x \left[\frac{Mn-k}{L} + KM \right] \qquad (6)$$

$$y[n + l] = \sum_{K_l=0}^{K_l^{max}} h_{lM+(K_l-[lM/L])L} x \left[\frac{Mn}{L} - K_l + \left[\frac{lM}{L} \right] \right] \qquad (7)$$

$$y[n + l] = \begin{bmatrix} h_{lM-[lM/L]L} \\ h_{lM-[lM/L]L+L} \\ \vdots \\ h_{lM+[(N-lM)/L]L} \end{bmatrix}^T \begin{bmatrix} x[m + \left\lfloor \frac{lM}{L} \right\rfloor] \\ x[m + \left\lfloor \frac{lM}{L} \right\rfloor - 1] \\ \vdots \\ x[m - \left\lfloor \frac{(N-lM)}{L} \right\rfloor] \end{bmatrix} \qquad (8)$$

$$y_{n,L} = H_{l \times (p+q+1)} x_{m+p,m-q} \qquad (9)$$

Where $y_{n,L}$, $H_{L*(p+q+1)}$, p, q and $x_{m+p,m-q}$ are:

$$y_{n,L} = \begin{bmatrix} y[n] & y[n+1] & y[n+2] & \ldots & y[n+L-1] \end{bmatrix}^T \qquad (10)$$

$$H_{L*(p+q+1)} = \begin{bmatrix} h_{-pL} & \cdots & h_{-L} & h_0 & h_L & \cdots & h_{(q-1)L} & h_{qL} \\ h_{M-pL} & \cdots & h_{M-L} & h_M & h_{M+L} & \cdots & h_{M+(q-1)L} & h_{M+qL} \\ h_{2M-pL} & \cdots & h_{2M-L} & h_{2M} & h_{2M+L} & \cdots & h_{2M+(q-1)L} & h_{2M+qL} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ h_{(L-1)M-pL} & \cdots & h_{(L-1)M-L} & h_{(L-1)M} & h_{(L-1)M+L} & \cdots & h_{(L-1)M+(q-1)L} & h_{(L-1)M+qL} \end{bmatrix} \qquad (11)$$

$$q = \lfloor N/L \rfloor \qquad p = \lfloor [(L-1)M]/L \rfloor \qquad h_k = 0, \text{ for } k < 0; k > N \qquad (12)$$

$$x_{m+p,m-q} = \begin{bmatrix} x[m+p] & x[m+p-1] & \ldots & x[m-q] \end{bmatrix}^T \qquad (13)$$

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2.3. *Properties of Matrix* $H_{L \times (p+q+1)}$

This section states three important properties in the relationships between the elements in the matrix $H_{L \times (p+q+1)}$.

(1) **Property 1:** The pth column in the matrix contains the following elements.

$$\tilde{h} = \begin{bmatrix} h_0 & h_M & h_{2M} & ...... & h_{(L-1)M} \end{bmatrix}^T \quad (14)$$

(2) **Property 2:** The lth row in the matrix $H_{L \times (p+q+1)}$ for $l = 0,1,...,L-1$ contains the μ_l^{th} polyphase component of the transfer function.

$$\mu_l = \mod(lM, L) \quad (15)$$

By denoting the number of zero valued coefficients before (after) the first (last) coefficient in the μ_l^{th} polyphase component with $\mu_\ell^{(b)}$ and $\mu_\ell^{(a)}$, they can be evaluated as

$$\mu_\ell^{(b)} = p - \left\lfloor \frac{\ell M}{L} \right\rfloor \quad (16)$$

$$\mu_\ell^{(a)} = q - \left\lfloor \frac{(N - \ell M)}{L} \right\rfloor \quad (17)$$

(3) **Property 3:** The matrix as given by (8c) can be expressed, in terms of the coefficients of the Nth order transfer function H(z), as

$$H_{L \times (p+q+1)} = \begin{bmatrix} h_0^{(H)} & h_1^{(H)} & ... & h_l^{(H)} & ... & h_{L-1}^{(H)} \end{bmatrix}^T \quad (18)$$

$$h_\ell^{(H)} = \begin{bmatrix} 0_{1,\mu_\ell^{(b)}} & h_{\mu\ell} & 0_{1,\mu_\ell^{(a)}} \end{bmatrix} \quad (19)$$

3. DESIGN ILLUSTRATIONS

In this section, two illustrative examples are provided to show how to efficiently exploit the coefficient symmetry of linear-phase FIR filters when using these filters for implementing the sampling-rate converters. First, a sampling rate converter by the rational factor 3/5 is studied and then 4/3 is presented. Along with this, implementation complexities (addition and multiplication) for both the cases are also studied.

3.1. *Rational Sampling-Rate Conversion By Factor 3/5*

This section considers a rational sampling-rate converter by a factor of L/M, as shown in Fig. 3.1, with $L = 3$, $M = 5$, and $N = 19$. In this case, the output sampling frequency is decreased by 5/3 with respect to the input sampling frequency.

$$p = \left\lfloor \frac{(L-1)M}{L} \right\rfloor = \left\lfloor \frac{10}{3} \right\rfloor = 3 \quad (20)$$

$$q = \left\lfloor \frac{N}{L} \right\rfloor = \left\lfloor \frac{19}{3} \right\rfloor = 6 \quad (21)$$

The relations between $L = 3$ consecutive output samples, and the input samples $x[m]$ is expressible in matrix form as shown in (22). In this expression, $n = 0, L, 2L,... = 0,3,6,...$ and the corresponding $m = (5/3)n = 0,5,10,...$.

Taking into account the filter coefficient symmetry, (22) may be rewritten as (23).

$$\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & h_0 & h_3 & h_6 & h_9 & h_{12} & h_{15} & h_{18} \\ 0 & 0 & h_2 & h_5 & h_8 & h_{11} & h_{14} & h_{17} & 0 & 0 \\ h_1 & h_4 & h_7 & h_{10} & h_{13} & h_{16} & h_{19} & 0 & 0 & 0 \end{bmatrix} x_{m+3,m-6} \quad (22)$$

$$\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & h_0 & h_3 & h_6 & h_9 & h_7 & h_4 & h_1 \\ 0 & 0 & h_2 & h_5 & h_8 & h_8 & h_5 & h_2 & 0 & 0 \\ h_1 & h_4 & h_7 & h_9 & h_6 & h_3 & h_0 & 0 & 0 & 0 \end{bmatrix} x_{m+3,m-6} \quad (23)$$

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$$H = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} c_{0,0} & c_{0,1} & c_{0,2} & c_{0,3} & c_{0,4} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & h_2 & h_5 & h_8 & h_8 & h_5 & h_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{0,4} & d_{0,3} & d_{0,2} & d_{0,1} & d_{0,0} \end{bmatrix} \begin{bmatrix} \mathbf{I}_5 & \mathbf{J}_5 \\ \mathbf{J}_5 & -\mathbf{I}_5 \end{bmatrix} \quad (24)$$

$$c_{0,0} = \frac{h_1}{2} \qquad d_{0,0} = -\frac{h_1}{2}$$

$$c_{0,1} = \frac{h_4}{2} \qquad d_{0,1} = -\frac{h_4}{2}$$

$$c_{0,2} = \frac{h_7}{2} \qquad d_{0,2} = -\frac{h_7}{2} \qquad\qquad (25)$$

$$c_{0,3} = \frac{h_0 + h_9}{2} \qquad d_{0,3} = \frac{h_0 - h_9}{2}$$

$$c_{0,4} = \frac{h_3 + h_6}{2} \qquad d_{0,4} = \frac{h_3 - h_6}{2}$$
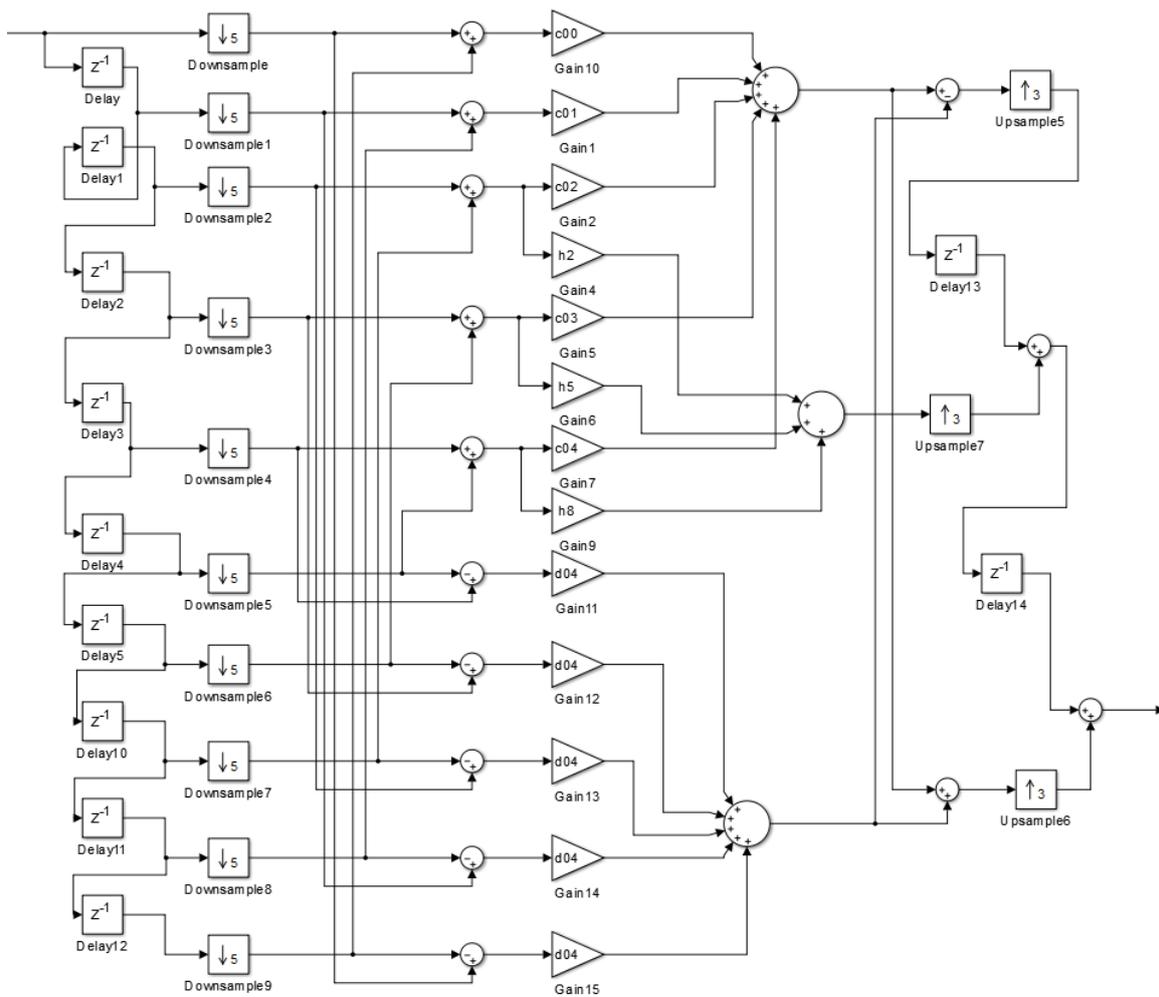
Fig. 2. Structure for a rational sampling rate converter by a factor 3/5

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The filter coefficient matrix is centro-symmetric matrix. Hence, it can be efficiently implemented by using the decomposition shown in (24). The structure for implementing this example is shown in Fig. 2. For generating three output samples, this implementation requires 13 multipliers and 20 adders. This corresponds to 4.3 multiplications and 6.6 additions per output sample.

3.2. Rational Sampling-Rate Conversion By Factor 4/3

This section considers a rational sampling-rate converter by a factor of L/M, as shown in Fig. 3.1,

with $L = 4$, $M = 3$, and $N = 21$. In this case, the output sampling frequency is increased by 4/3 with respect to the input sampling frequency.

$$p = \left\lfloor \frac{(L-1)M}{L} \right\rfloor = \left\lfloor \frac{9}{4} \right\rfloor = 2 \tag{26}$$

$$q = \left\lfloor \frac{N}{L} \right\rfloor = \left\lfloor \frac{21}{4} \right\rfloor = 5 \tag{27}$$

$$\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \\ y[n+3] \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_0 & h_4 & h_8 & h_{12} & h_{16} & h_{20} \\ 0 & 0 & h_3 & h_7 & h_{11} & h_{15} & h_{19} & 0 \\ 0 & h_2 & h_6 & h_{10} & h_{14} & h_{18} & 0 & 0 \\ h_1 & h_5 & h_9 & h_{13} & h_{17} & h_{21} & 0 & 0 \end{bmatrix} x_{m+2, m-5} \tag{28}$$

$$\begin{bmatrix} y[n] \\ y[n+1] \\ y[n+2] \\ y[n+3] \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_0 & h_4 & h_8 & h_9 & h_5 & h_1 \\ 0 & 0 & h_3 & h_7 & h_{10} & h_6 & h_2 & 0 \\ 0 & h_2 & h_6 & h_{10} & h_7 & h_3 & 0 & 0 \\ h_1 & h_5 & h_9 & h_8 & h_4 & h_0 & 0 & 0 \end{bmatrix} x_{m+2, m-5} \tag{29}$$

$$H = \begin{bmatrix} \mathbf{I}_2 & \mathbf{J}_2 \\ \mathbf{J}_2 & -\mathbf{I}_2 \end{bmatrix} \begin{bmatrix} c_{0,0} & c_{0,1} & c_{0,2} & c_{0,3} & 0 & 0 & 0 & 0 \\ 0 & c_{1,1} & c_{1,2} & c_{1,3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & d_{1,3} & d_{1,2} & d_{1,1} & 0 \\ 0 & 0 & 0 & 0 & d_{0,3} & d_{0,2} & d_{0,1} & d_{0,0} \end{bmatrix} \begin{bmatrix} \mathbf{I}_4 & \mathbf{J}_4 \\ \mathbf{J}_4 & -\mathbf{I}_4 \end{bmatrix} \tag{30}$$

$$
\begin{aligned}
c_{0,0} &= \frac{h_1}{2} & d_{0,0} &= -\frac{h_1}{2} \\
c_{0,1} &= \frac{h_5}{2} & d_{0,1} &= -\frac{h_5}{2} \\
c_{0,2} &= \frac{h_0 + h_9}{2} & d_{0,2} &= \frac{h_0 - h_9}{2} \\
c_{0,3} &= \frac{h_4 + h_8}{2} & d_{0,3} &= \frac{h_4 - h_8}{2} \\
c_{1,1} &= \frac{h_2}{2} & d_{1,1} &= -\frac{h_2}{2} \\
c_{1,2} &= \frac{h_3 + h_6}{2} & d_{1,2} &= \frac{h_3 - h_6}{2} \\
c_{1,3} &= \frac{h_7 + h_{10}}{2} & d_{1,3} &= \frac{h_7 - h_{10}}{2}
\end{aligned}
\tag{31}
$$

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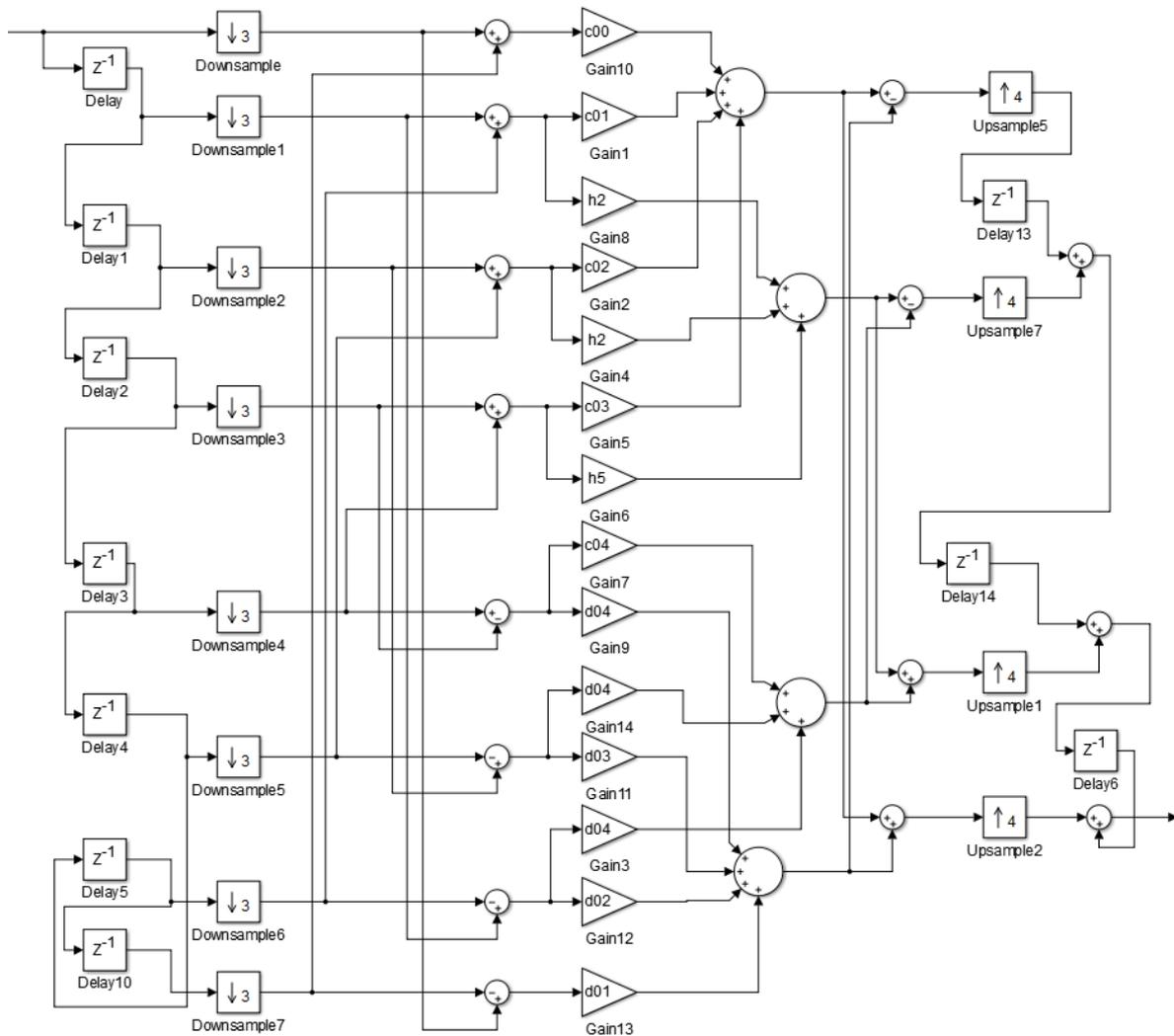*Available online at www.ijrat.org*

Fig. 3. Structure for a rational sampling rate converter by a factor 4/3

The relations between $L = 4$ consecutive output samples, and the input samples $x[m]$ is expressible in matrix form as shown in (28). In this expression, $n = 0, L, 2L, \ldots = 0, 4, 8, \ldots$ and the corresponding $m = (3/5)n = 0, 3, 6, \ldots$.

Taking into account the filter coefficient symmetry, (28) may be rewritten as (29). The filter coefficient matrix is centro-symmetric matrix. Hence, it can be efficiently implemented by using the decomposition shown in (30). The structure for implementing this example is shown in Fig. 3. For generating 4 output samples, this implementation requires 14 multipliers and 22 adders. This corresponds to 3.5 multiplications and 5.5 additions per output sample.

4. IMPLEMENTATION COMPLEXITY COMPUTATION

The proposed method for achieving efficient implementation of the system simultaneously taking into account the coefficient symmetry given by is divided into three cases. The first two cases, which are referred to as Cases A and B, respectively, consider rational sampling-rate converters with special relations between the parameters N, M and L whereas the third case, referred to as Case C, shows how a system with any combination of N, M and L and can be converted to those two special cases in such manner that an efficient implementation is achieved also in this general case.

First, the implementation complexities are estimated for Case A and B converters, and then, based on these complexity estimates, it is explained how to estimate the complexity for Case C converters. In all cases,

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C_p^* and C_p^+ stand for the number of multiplications and the number of additions per output sample, respectively.

4.1. Case A

This section concentrates on rational sampling-rate converters, for which the filter order is given by $N = M(L-1) + (2k+1)L$ where is k an integer. For these converters, the general form of input–output relations is expressible as

$$\mathbf{y}_{n,L} = \mathbf{H}_{L \times (p+q+1)} \mathbf{x}_{m+p,m-q} = \mathbf{H}_A \mathbf{x}_{m+p,m-q} \quad (32)$$

where the size of the matrix $\mathbf{H}_A$ is L_H by 2λ.

$$L_H = L \quad \text{and} \quad \lambda = \frac{p+q+1}{2} \quad (33)$$

The implementation complexity of the matrix H_A can be estimated by (34) and (35).

$$C_p^* = C_A^* = \lambda \quad (34)$$

$$
C_p^+ = C_A^+
= \begin{cases} \lambda + \dfrac{2\lambda}{L_H} - \dfrac{\mod(L_H,2)}{L_H} & \text{for } L_H > 1 \\ 2\lambda - 1 & \text{for } L_H = 1 \end{cases} \quad (35)
$$

4.2. Case B

This section concentrates on rational sampling-rate converters, for which the filter order is given by $N = M(L-1) + 2kL$ where is k an integer. For these converters, the general form of input–output relations are expressible as

$$
\mathbf{y}_{n,L} = \mathbf{H}_{L \times (p+q+1)} \mathbf{x}_{m+p,m-q} \\
= \mathbf{h}_B \mathbf{x}_{m-\lambda+p} + \mathbf{H}_B \begin{bmatrix} \mathbf{x}_{m+p,m+p-\lambda+1} \\ \mathbf{x}_{m+p-\lambda-1,m-q} \end{bmatrix} \quad (36)
$$

where the size of the matrix $\mathbf{H}_B$ is L_H by 2λ and the vector $\mathbf{h}_B$ of length L_H with

$$L_H = L \quad (37)$$

$$\lambda = \frac{p+q+1}{2} \quad (38)$$

The implementation complexity for this case can be estimated by (39) and (40).

$$C_p^* = C_B^* = \lambda + \frac{1}{L_H}\left\lfloor \frac{L_H}{2} \right\rfloor \quad (39)$$

$$
C_p^+ = C_B^+ \\
= \begin{cases} \lambda + \dfrac{2\lambda}{L_H} + 1 - \dfrac{\mod(L_H,2)}{L_H} & \text{for } L_H > 1 \\ 2\lambda & \text{for } L_H = 1 \end{cases} \quad (40)
$$

4.3. Case C

This section concentrates on rational sampling-rate converters, for which the filter order N is arbitrary and does not depend on L and M.

In order to arrive at an efficient implementation also for these converters, it is advantageous to separate the input–output transfer matrix $H_{L \times (p+q+1)}$ into two matrices H_{C1} and H_{C2} as follows:

$$H_{L \times (p+q+1)} = \begin{bmatrix} 0_{L_1, p-p1} & H_{C1} \\ H_{C2} & 0_{L_2, q-q_2} \end{bmatrix} \quad (41)$$

where the matrices H_{C1} and H_{C2} are of sizes $L_1 \times (q + p_1 + 1)$ and $L_2 \times (q_2 + p + 1)$, respectively.

$$
y_{n,L_1} = H_{C1} x_{m+p_1, m-q} \\
y_{n+L_1, L_2} = H_{C2} x_{m+p, m-q_2} \quad (42)
$$

The implementation complexity for Case C converters can thus be evaluated as

$$C_p^* = \frac{L_1 C_{H_{C1}}^* + L_2 C_{H_{C2}}^*}{L} \quad (34)$$

$$C_p^+ = \frac{L_1 C_{H_{C1}}^+ + L_2 C_{H_{C2}}^+}{L} \quad (35)$$

Where the implementation complexities of H_{C1} and H_{C2} are evaluated by computing complexities of H_A and H_B, respectively. In order to evaluate the complexity of Case C converters, first, the matrix

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separation has to be performed and then, depending on the resulting separation, the complexities of the matrices and are accordingly evaluated.

5. RESULTS

In this section, computed implementation complexities for sampling rate converters discussed in section 3 are presented. To develop a comparative analysis, two more techniques are considered while computing addition and multiplication complexities; fast-Fourier-transform (FFT) based cyclic algorithm [8] and polyphase implementation [9].

5.1. *Rational Sampling Rate Conversion By Factor 3/5*

Sampling rate conversion by a factor 3/5 is shown in Fig. 4. The original signal samples are 50. After applying fractional sampling rate converter of 3/5, the

signal samples are modified to 30. As can be seen from Fig. 5, number of additions in poly-phase and proposed structure do not differ much. In the figure, N is the filter order. C^+p stands for Number of Multiplications in Proposed Implementation. C^+_d stands for Number of Multiplications in poly-phase Implementation.

Fig. 6 shows that number of multiplications in poly-phase implementation is more than the number of multiplications in proposed implementation. $C*p$ stands for Number of Multiplications in Proposed Implementation. $C*d$ stands for Number of Multiplications in poly-phase Implementation.

For lower values of N the relative complexity of the proposed implementation is high. As the value of N increases the relative complexity of the proposed implementation is lowered. This can be observed from Table 1.
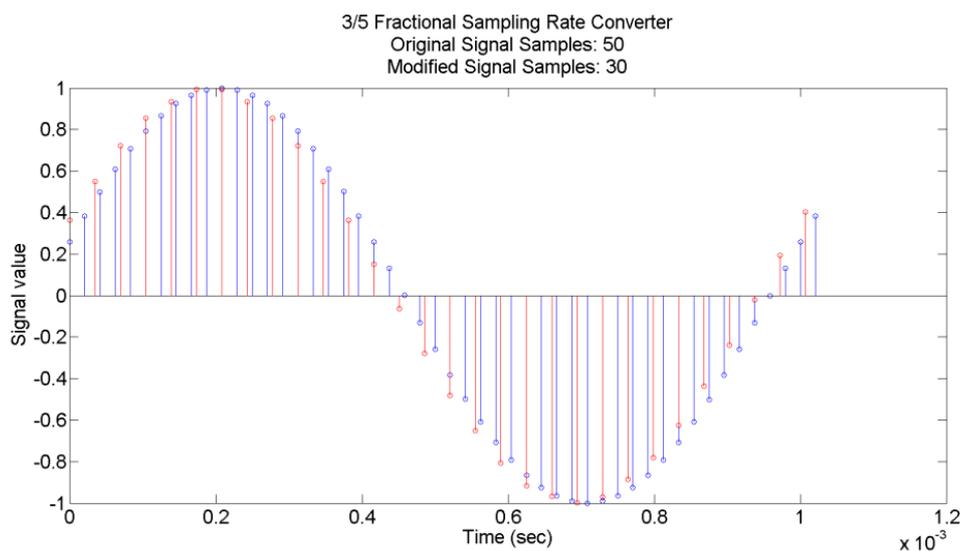

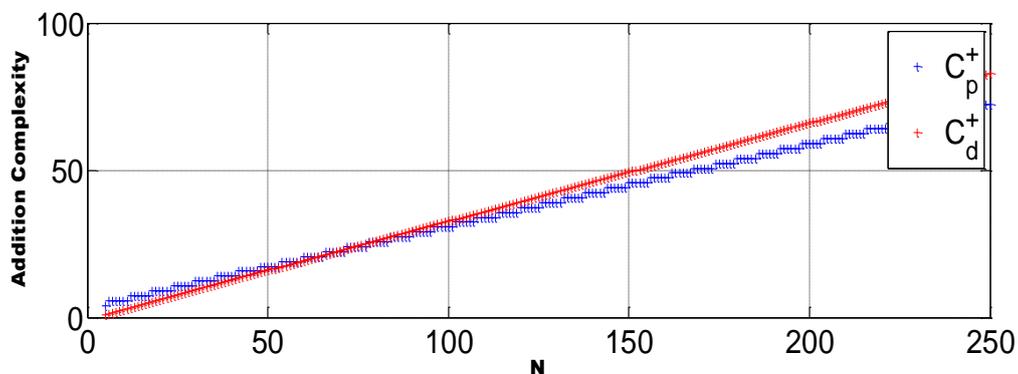Fig. 4. Sampling Rate Conversion by 3/5 Output

Fig. 5. Comparison of Poly-phase and Proposed Structure with respect to Addition Complexity

International Journal of Research in Advent Technology, Vol.5, No.3, March 2017
E-ISSN: 2321-9637
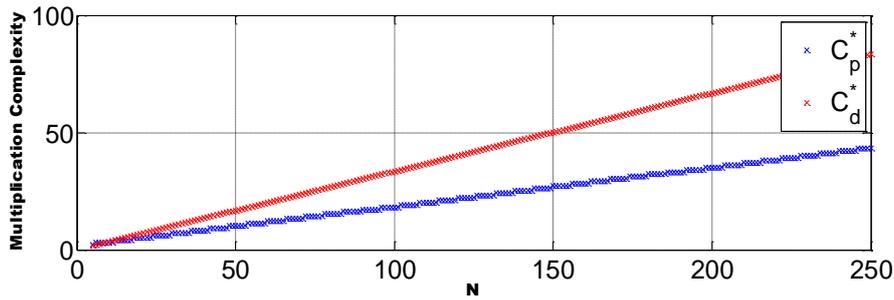*Available online at www.ijrat.org*

Fig. 6. Comparison of Poly-phase and Proposed Structure with respect to Multiplication Complexity
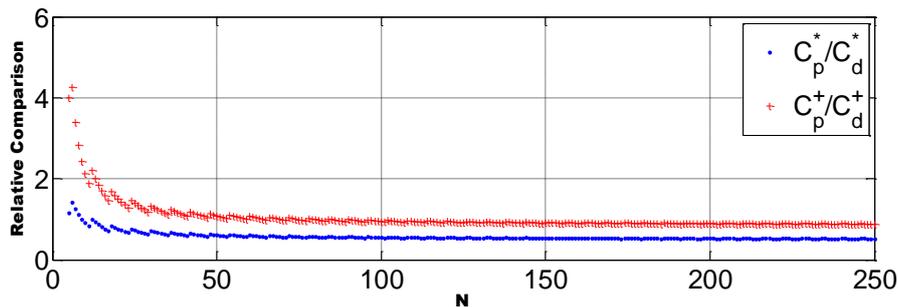

Fig. 7. Relative Comparison between Proposed and Poly-phase Implementation

Table 1. Implementation complexity for rational sampling-rate converters by 3/5 for the proposed and poly-phase implementation

		Proposed		Polyphase		Comparison			
Case	N	Cp*	Cp+	Cd*	Cd+	Case	N	Cp*/Cd*	Cp+/Cd+
A	211	37	61.33333	70.66667	69.66667	A	211	0.523585	0.880383
B	214	37.33333	62.33333	71.66667	70.66667	B	214	0.52093	0.882075
C	23	4.333333	8	8	7	C	23	0.541667	1.142857
C	209	35.33333	70	70	69	C	209	0.504762	1.014493
C	210	36	71.66667	70.33333	69.33333	C	210	0.511848	1.033654
C	212	36	71.33333	71	70	C	212	0.507042	1.019048
C	213	36.33333	72.33333	71.33333	70.33333	C	213	0.509346	1.028436

(Number of multiplications (C*) and Additions (C+) per output sample)

5.2. *Rational Sampling Rate Conversion By Factor 4/3*

Sampling rate conversion by a factor 4/3 is shown in Fig. 8. The original signal samples are 60. After applying fractional sampling rate converter of 4/3, the signal samples are modified to 80. As can be seen from Fig. 9, number of additions in poly-phase and proposed structure do not differ much. In the figure, N

is the filter order. C_p^+ stands for Number of Multiplications in Proposed Implementation. C_d^+ stands for Number of Multiplications in poly-phase Implementation.

Fig. 10 shows that number of multiplications in poly-phase implementation is more than the number of multiplications in proposed implementation. C_p^* stands for Number of Multiplications in Proposed

International Journal of Research in Advent Technology, Vol.5, No.3, March 2017
E-ISSN: 2321-9637
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Implementation. $C*d$ stands for Number of Multiplications in poly-phase Implementation.

For lower values of N the relative complexity of the proposed implementation is high. As the value of N increases the relative complexity of the proposed implementation is lowered. This can be observed from Table 2.

Fig. 12 (a) shows that the ratio of number of multiplications in FFT based cyclic algorithm $C*13$ and poly-phase implementation is greater than the ratio of number of multiplications of proposed implementation and poly-phase implementation. Fig. 12 (b) shows that the addition complexity for the ratio of FFT based cyclic algorithm $C+13$ and poly-phase implementation is less than the addition complexity for the ratio of proposed and poly-phase implementation.

6. CONCLUSION

This research work presents the design and implementation scheme of rational sampling rate converter utilizing symmetric technique. An efficient structure is designed for sampling rate converter having rational factor L/M. All results are carried out using MATLAB simulation. The proposed design gives better performance and less complexity as compared to polyphase.

The proposed optimized design shows that symmetric FIR filter require 50% less hardware as compare to transposed FIR structure. This concludes that low-pass FIR filters are the right choice due to their stability and linearity. Moreover, it is concluded that the filter structure should be of a symmetric type since this reduces the amount of multiplications. Symmetric technique reduces around 50% complexity as compare to polyphase. It is observed from examples that for different values of L, M and N, Implementation complexity varies. For high values of L and M, high order of FIR filters are required which are difficult to design.

The proposed method can be used to implement the converter in a more efficient way than the corresponding polyphase implementation for any combination of values M, L and N. However it should be mentioned that for large values of M and L, the proposed method as well as the polyphase one might get impractical due to high hardware requirements (number of delays, number of multipliers, number of required bits, etc.). In cases when both M and L can be factorized, this problem can be overcome by using multistage rational sampling rate converters.
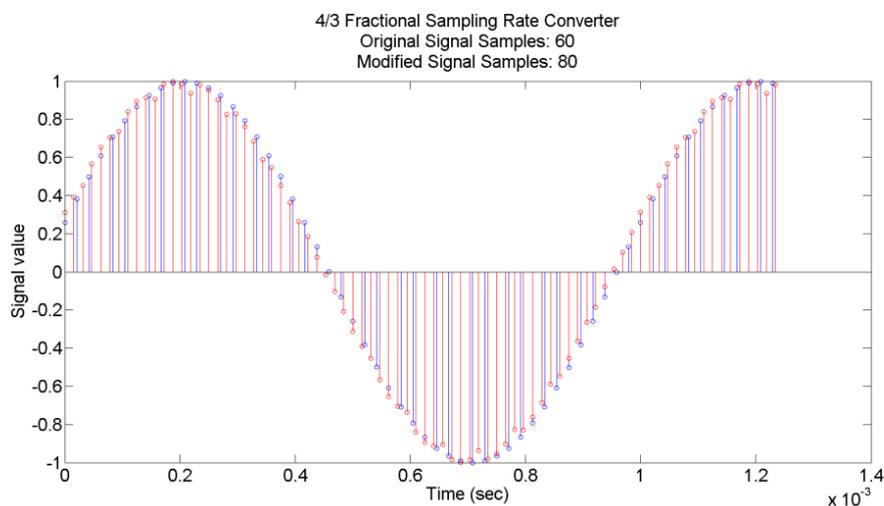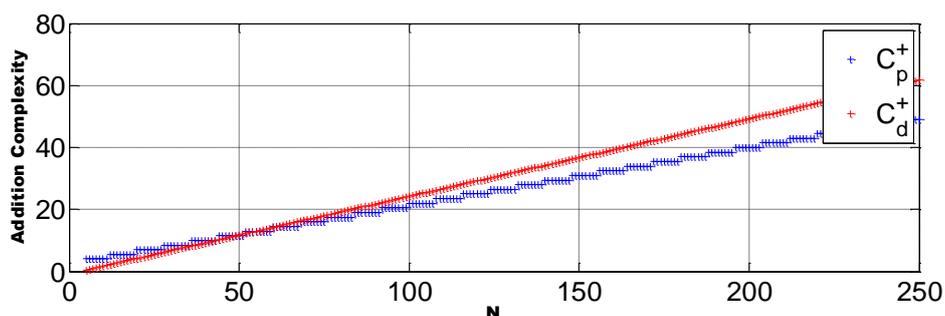

Fig. 8. Sampling Rate Conversion by 4/3 Output

Fig. 9. Comparison of Poly-phase and Proposed Structure with respect to Addition Complexity

International Journal of Research in Advent Technology, Vol.5, No.3, March 2017
E-ISSN: 2321-9637
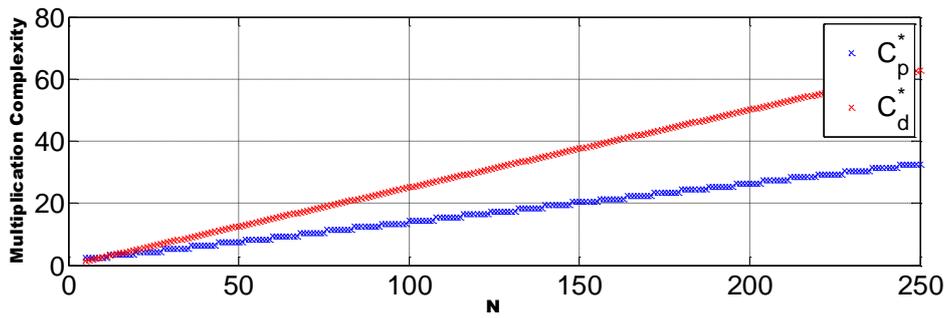*Available online at www.ijrat.org*

Fig. 10. Comparison of Poly-phase and Proposed Structure with respect to Multiplication Complexity
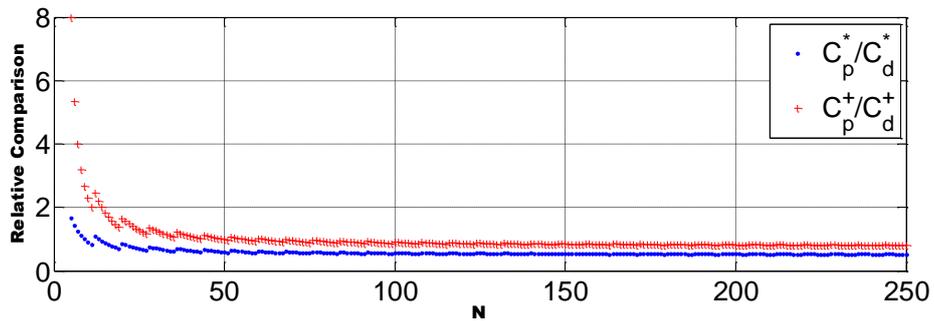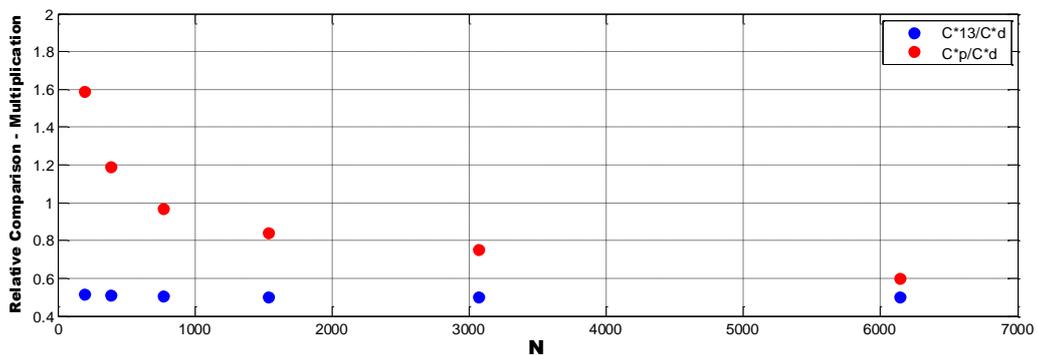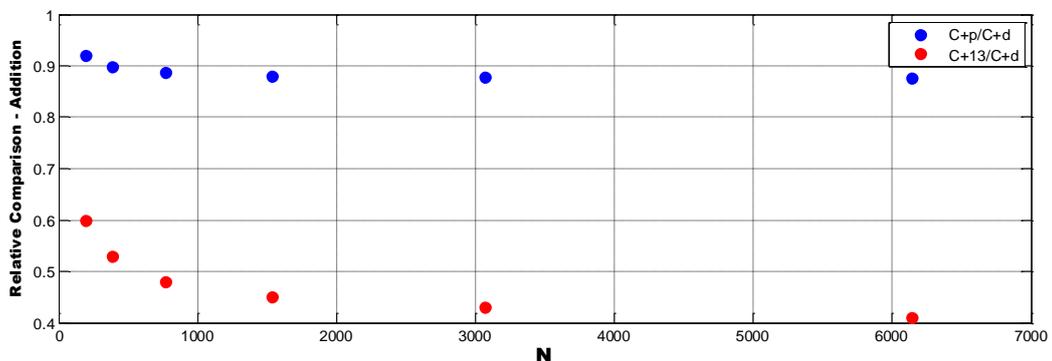

Fig. 11. Relative Comparison between Proposed and Poly-phase Implementation

(a)

(b)

Fig. 12. Comparison between complexities of the proposed implementation and FFT based cyclic algorithm
(a) Number of Multiplications (b) Number of Additions

Table 2. Implementation complexity for rational sampling-rate converters by 4/3 for the proposed and poly-phase implementation

International Journal of Research in Advent Technology, Vol.5, No.3, March 2017
E-ISSN: 2321-9637
Available online at www.ijrat.org

		Proposed		Polyphase		Comparison			
Case	N	Cp*	Cp+	Cd*	Cd+	Case	N	Cp*/Cd*	Cp+/Cd+
A	213	22	30.6	42.8	41.8	A	213	0.5140	0.7320
B	209	22.4	31.6	42	41	B	209	0.5333	0.7707
C	23	3	5	4.8	3.8	C	23	0.6250	1.3158
C	210	22.2	35.4	42.2	41.2	C	210	0.5261	0.8592
C	211	21.93	39.07	42.4	41.4	C	211	0.5173	0.9436
C	212	21.87	38.93	42.6	41.6	C	212	0.5133	0.9359
C	214	21.93	39.07	43	42	C	214	0.5100	0.9301

(Number of multiplications (C*) and Additions (C+) per output sample)

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