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A Survey on Test pattern compression Techniques in Analog and Mixed signal circuits

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Abstract: Testing of modern IC devices involves three process: 1. Test pattern generation, 2. Test pattern compaction, 3. Test pattern application. Test patterns are generated in first phase, compressed in second phase and applied to DUT (Device under Test). The response of DUT is compared with actual response in order to analyze the device's behaviors. Earlier part of modern device evolves with digital circuits. But most of modern IC's in today's technology comes with both analog (ADC) and digital elements (DAC). There are many scheme's has been developed for digital circuits than analogue circuits. Testing of analogue circuits are more difficult than digital circuits since the analog test involves more parameter than digital testing. So there is need of efficient test compression. The survey of this paper is focused on test compression techniques and its analysis on methodology, test patterns, run time on various analogue & mixed signal circuits.

Index Terms—ADC, DAC Functional test, Fault Tolerance, Test Patterns.

I. INTRODUCTION

The designer has integrated both analogue and digital circuits in a single chip in order to reduce the cost. This types of IC's are called as Mixed signal IC' and used in many applications like Telecommunication, multimedia, networking, process control and real time control systems[1]. The main components of these systems are ADC and DAC. The analogue signal are converted in to digital and interfaced to digital chip portions. Due to this nature, testing of mixed signal circuit is a complex task. Testing cost, test application time is very high compared digital circuits. To reduce the test application time, several test compression method has been evolved for both digital and analog circuits. This survey paper analyzed the different techniques to reduce run time of analogue and mixed signal circuits.

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II. LITERATURE SURVEY AND RELATED WORKS

[2].The Author try to reduce the misclassification of good device as a faulty device by reducing the quantization level and choose of proper sampling point based on tolerance band.

[3]The Author proposed two approaches to reduce the run time without sacrificing the accuracy. The two approaches are DC verification and transient analysis. These approaches are applied on discretized model of analogue and mixed signal circuits with help of SAT solver.

[4]The author follows two approach to improve the quality of test in Motorola's AMS chip. One approach is converting; analogue input to digital input during test mode and the other is on chip test compression using MISR. Multiple Input Signature Register (MISR) is used to reduce the output pins.

[5]The Author presented the generalised approach for testing analogue and mixed signal circuit. The author used ternary logic to represent the signature (+,-, 0)that applied directly to ADC and DAC device to analyse the parameters SNR and THD.

[6]The author used UBISTA (Unified Built In Self-Test Approach) to test the analogue circuit, by converting transient response of analogue circuit into equivalent digital bits and it was given to Parallel input LFSR to generate digital signature.

The analogue to digital conversion and LFSR based signature analysis techniques leads to compression techniques for analogue and mixed signal circuits.

[7].Testing cost of analogue and mixed signal is high due its design complexity. The test effectiveness of mixed signal circuits depends on both its functional and structural test. The author proposed a new approach to compress the faults and tried to reduce the simulation time. Test compaction achieved through equivalent fault detection and collapsing on the fault list. Representative faults are defined in analogue cells based on their similarity and functional response. Structural fault model includes stuck on stuck off faults in MOS devices. Once the test stimuli's are generated, they are classified and clustered based on the response. [8]

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S. No	Paper Title	Authors	Methodology / Device Approach	Techniques	Algorithms Proposed / Used	Results Discussed
1.	Robust Data Compression For Analogue Test Output[2]	Aleksandra Rankov, Gaynor E. Taylor , John Webster	Hybrid Built-In Self-Test (HBIST) for Mixed Analogue/Digital Integrated Circuits	Reducing The Quantization Level and Selection of Proper Sampling Point Based On Tolerance Band	No	Reduction in Run Time.
2.	Verification of Analogue and Mixed-Signal on Discretized Models [3]	Dr. Henry Selvaraj, Nikita Ramesh Wanjale	A Ring Oscillator-DC Verification Tunnel Diode Oscillator-Transient Analysis	DC Verification And Transient Analysis, Using Satisfiability Solvers	Yes	Reduction in Run Time
3.	Using On-chip Test Pattern Compression For Full Scan SoC Designs[4]	Helmut Lang, Jens Pfeiffer, Jeff Maguire	Motorola's SoC	Reduction of number of inputs and output pin	ISAT -Satisfiability Solver	Fault Coverage Improved by 4 %
4.	Performance Characterization of Mixed-Signal Circuits Using a Ternary Signal Representation[5]	Hak-sooYu, Hongjoong Shin, Ji Hwan (Paul) Chun and Jacob A. Abraham	Built-In Self-Test (Ternary logic BASED) - General Mixed - Signal Circuits	Used Ternary Representation Logic, Dynamic Performance Characteristics of ADC & DAC are analyzed	No	SNR, THD
5.	Digital Data Compression Techniques For Analogue Blocks In Mixed Signal Devices[6]	Hak-soo Yu, Hongjoong Shin, Ji Hwan (Paul) Chun and Jacob A. Abraham	UBISTA (Unified Built-In Self-Test Approach) CMoS Operational Amplifiers	Digital Version of Transient response and Parallel LFSR	No	Compression occurs without any loss in fault coverage
6.	Analogue and Mixed-Signal Production Test Speed Up by means of fault list compression.[7]	NunoGuerreiro Marcelino Santos and Paulo Teixeira	DC – DC Converter	Reducing the fault list	No	Reduction in the simulation time
7.	On-Chip Analog Output Response Compaction [8]	M.Renovell, F. Azdis&Y.B Ertrand	4^{th} Order Sallen Key Filter	Cumulative Adder based Test Response Compression	No	Fault coverage improved
8.	Optimal Choice of Arithmetic Compactors for Mixed-Signal Systems[9]	Vadim Geurkov	3 Bit ADC	Proposed Low Cost Compaction Circuit	No	Reduced distortion
9.	Self-organized A VLSI Neural Processor for Image Data Compression [10]	Wai-Chi Fang, Bing J. Sheu, Oscal T.-C. Chen, and Joongho Choi	-	Developed a Neural Processor	No	Low power and reduced pin count processor is achieved with intrinsic compression ratio of 33

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The author discussed two exiting approach and its demerits also proposed a multi input signature analyser to monitor both voltage and current. The integrator used to reduce the test response of the mixed signal circuit.

[9]. The author introduced a low cost compactor with low aliasing rate for both off chip and on-chip analogue and mixed signal circuit. The low cost compactor designed with algebraic and arithmetic modulus circuit.

[10].The author developed a neural network for both speech and image applications. The two main blocks of neural processor are pipelined codebook generator and a paralleled vector quantizer. The author used parallel vector quantizer for compression purpose. Quantization process of each input vector is done by vector quantizer in neural processor.

III. CONCLUSION

Testing of analogue & mixed signal circuit is a challenging one due to its internal circuit complexity. Existing algorithms and test methodology suits only for digital circuits. Most of the current research work is mainly focused in the area of testing, verification and compression of analogue and mixed signal circuits. This survey paper on test pattern reduction (compression) in order to speed up the testing time of analogue circuits. It's concluded that, new fault models, efficient test algorithms and test methodology need to be developed to improve fault coverage and compression techniques.

REFERENCES

[1] M. Bushnell and V. Agrawal, Essentials of Electronic Testing for Digital, MemoryandMixed Signal VLSI Circuits, Kluwer, 2000.
[2] A. Rankov, G.E. Taylor, J. Webster, "Robust data compression for analogue test outputs", Proceedings of the Eighth IEEE International On-Line Testing Workshop (IOLTW 2002)Year: 2002
[3] Henry Selvaraj , Nikita Ramesh Wanjale, "Analog and Mixed-Signal Verification Using Satisfiability Solver on Discretized Models", 25th International Conference on Systems Engineering (ICSEng) Year: 2017
[4] H. Lang, J. Pfeiffer , J. Maguire, "Using on-chip test pattern compression for full scan SoC designs", Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159)Year: 2000
[5] Hak-Soo Yu, H. Shin, J.H. Chun, J.A. Abraham, "Performance characterization of mixed-signal circuits using a ternary signal representation," 2004 International Conference on TestYear: 2004
[6] G.E. Taylor, J. Webster ,P. Skladel , P. Simek, D.E,"Digital data compression techniques for analogue blocks in mixed signal devices", IEE Colloquium on Testing Mixed Signal Circuits and Systems (Ref. No: 1997/361) Year: 1997
[7] NunoGuerreiro ,Marcelino Santos , Paulo Teixeira "Analogue and Mixed-Signal Production Test Speed-Up by Means of Fault List Compression" Circuits and Systems Year: 2013
[8] M. Renovell , F. Azais , Y. Bertrand, "On-chip analog output response compaction, " Proceedings European Design and Test Conference. ED & TC 97 Year: 1997
[9] Vadim Geurkov" Optimal choice of arithmetic compactors for mixed-signal systems, " IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems Year: 2012
[10] Wai-Chi Fang, Bing J. Sheu, Oscal T.-C. Chen, and Joongho Choi, "A VLSI Neural Processor for Image Data Compression Using Self-organization Networks"IEEE Transactions on Neural Networks Year: 1992, Volume: 3, Issue: 3 , Pages: 506 - 518

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